MODEL 1260A

PULSING TEST SET

SERVICE

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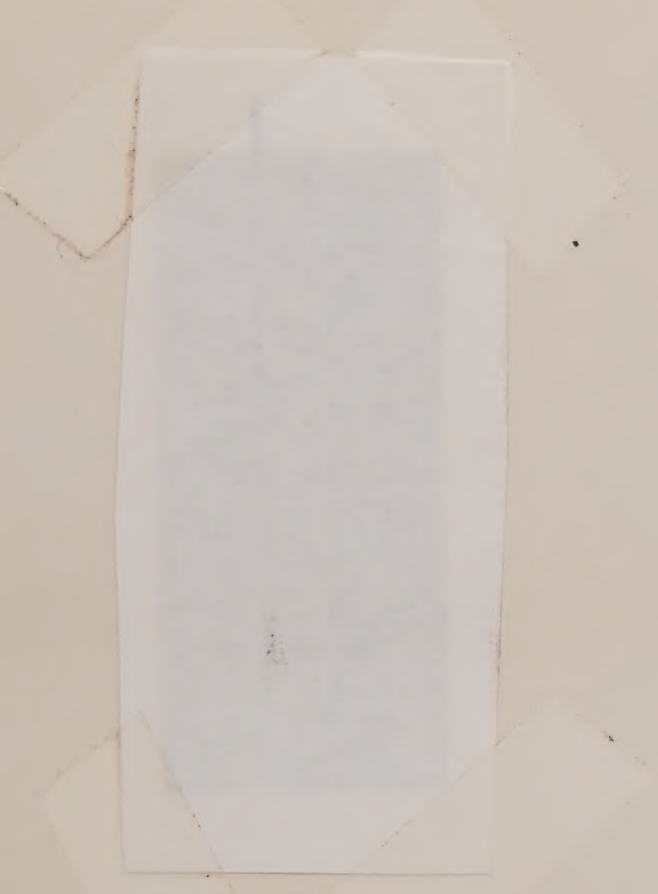

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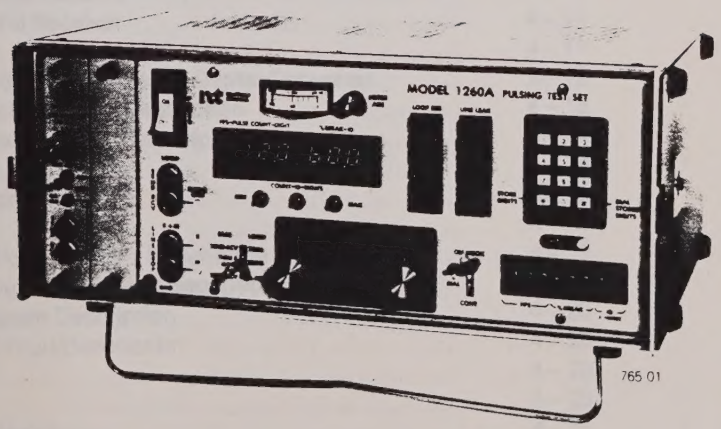

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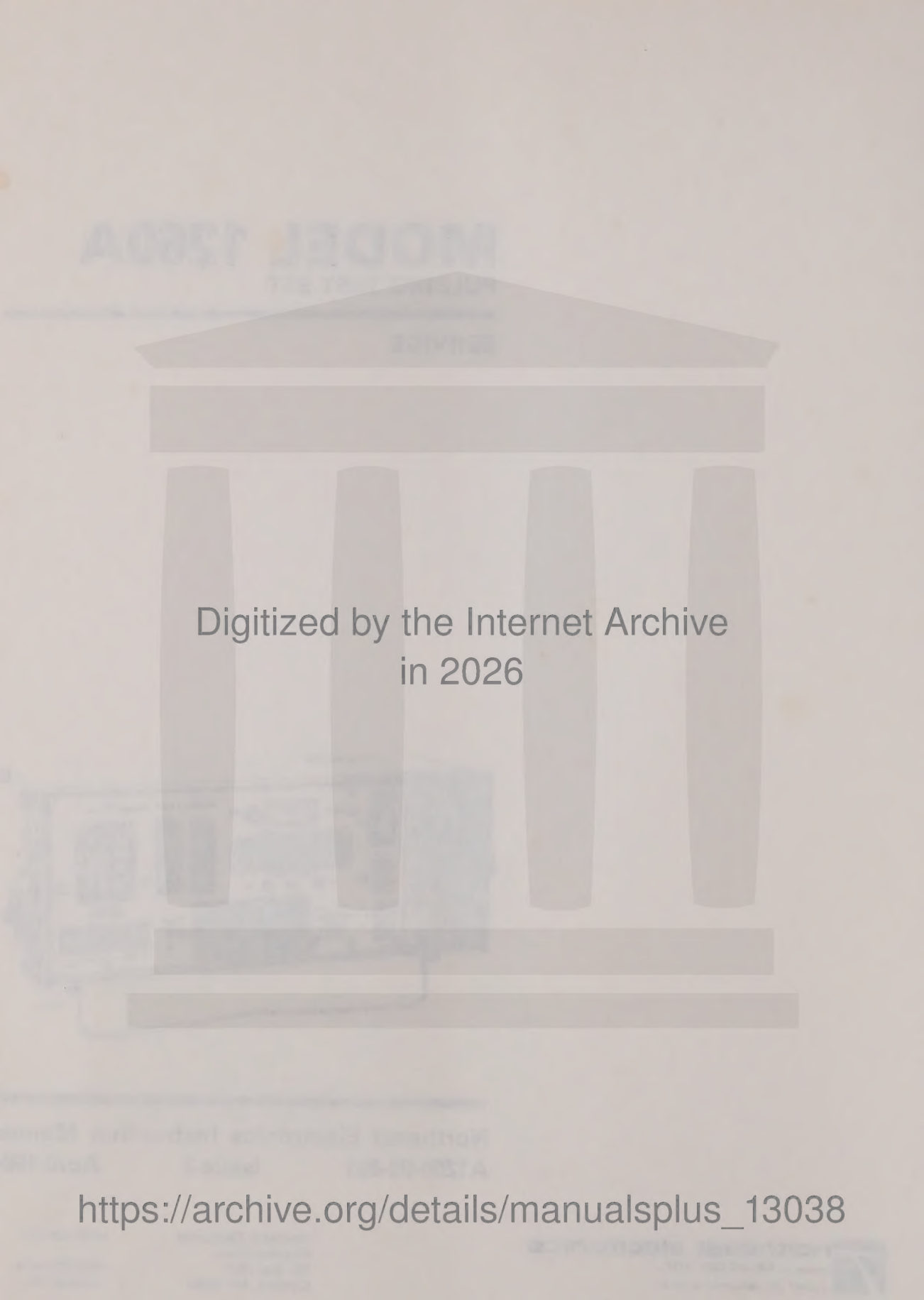
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SECTION 1

GENERAL DESCRIPTION

1.1 This manual describes the Northeast Electronics Model 1260A Pulsing Test Set. The test set is a precision digital instrument designed to send, receive, and measure pulsing in any of several loop, E&M and SF modes. The sending and receiving capabilities are fully independent so mixed modes can be used...for example, sending loop while receiving E&M, or vice versa.

1.2 The send section transmits continuous pulsing, or any number of dialed digits. Alternatively, a user-programmed number up to 16 digits long can be automatically dialed or redialed from memory. Digits are entered via a front panel keypad. Outpulsing speed, percent break, and interdigit time are precisely variable over wide limits to permit easy, but exact margin testing. Selectable loop resistance and line leak networks are built in for convenient loop simulation and margining as needed.

1.3 The receive section precisely measures the speed, percent break, and interdigit time of received pulsing. No pre-measurement calibration is required. Measurement results are displayed on a digital readout.

1.4 The Model 1260A gives its user the following measurement data:

- ☐ Average speed and percent break over multiple pulses in a string (continuous pulsing or one or more dialed digits);
- ☐ Minimum speed and percent break for pulses in a string (slowest speed and lowest percent break);
- ☐ Maximum speed and percent break for pulses in a string (fastest speed and highest percent break);
- ☐ Total count of all pulses received for multiple pulses/digits in a string (up to a maximum of 999 pulses);
- ☐ Minimum interdigit time for digits in a string; and
- ☐ Display of each individual digit received and the actual interdigit time following that digit (up to 16 digits maximum).

1.5 The 1260A measurement data helps reveal common signaling problems such as: (a) first pulse problems from A-relays; (b) split (double) pulsing and other erratic relay operations; and (c) intermittent signaling conditions of other types.

1.6 A digital readout precisely displays measurement data. An analog meter is also included to show short-term percent break variations and on-hook/off-hook status on the line. The analog meter indications are the same for all loop, E&M, and SF modes.

1.7 TYPICAL APPLICATIONS

1.8 The Model 1260A can pulse test both signaling and switching equipment. It has the capabilities needed for:

- ☐ Acceptance testing of new plant;
- ☐ Routine and margin testing of in-service plant;
- ☐ Trouble sectionalizing; and
- ☐ Alignment/tune-up adjustments.

1.9 The 1260A simplifies the task of exercising circuits over their ranges of sectional and end-to-end signaling requirements. Margin tests for speed, percent break, interdigit time, leak impedance and loop resistance can all be performed using the 1260A's built-in features.

1.10 The 1260A is also suitable for pulse testing/tuning a variety of signaling and switching components such as:

- ☐ Registers and senders;
- ☐ Pulse repeaters;
- ☐ Pulse correctors;
- ☐ Loop to/from E&M converters; and
- ☐ Switch train components . . . digit absorbing selectors, regular selectors, connectors, and related equipment.

1.11 The instrument's ability to display each received digit and the interdigit time for that digit is particularly useful in identifying problems associated with senders, repeaters, and similar equipment. And, the independent send and receive functions permit easy checks on the accuracy of many signaling converters. That is, exact input-to-output comparisons can be made on loop to E&M converters, loop to SF converters, and so forth.

1.12 Dynamic testing can be performed on A-relays under realistic conditions which closely approximate those existing in service.

1.13 The Model 1260A can make pulsing measurements under a wide variety of conditions. For example, the instrument will maintain full pulsing speed and percent break accuracy when making terminated measurements in the presence of contact suppression networks; up to 2 microfarads and 600 ohms. (This often eliminates the need for removing such networks.) Also, "live" pulsing can be monitored on in-service circuits by bridging the line.

1.14 TEST MODE SELECTION

1.15 The independent send and receive sections handle the following types of signaling arrangements:

- ☐ Dry loop;
- ☐ Wet loop (battery and ground);
- ☐ E-lead ground and open pulsing (employed by E&M Types I, II, and III);
- ☐ E-lead ground battery pulsing;
- ☐ M-lead battery and open pulsing (employed by E&M Type II signaling);
- ☐ M-lead battery and ground pulsing (employed by E&M Types I and III); and
- ☐ SF (2600 Hz).

1.16 For wet loop pulsing, the 1260A makes/breaks both sides of the line. This is an important factor in some applications. A convenient test A-relay in the 1260A is easily substituted for an in-circuit A-relay when required by loop testing practices.

1.17 For E&M testing at six-wire patch bays or similar points, the 1260A's internal design makes it possible to easily select the proper conditions for sending/receiving in either the line or drop directions. Idle/busy status indicators and a reverse direction busy-out feature are also built in for E&M testing.

1.18 SEND SECTION

1.19 The Model 1260A has a precision, crystal-controlled oscillator as the master reference for all outpulsing. Outpulsing speed is variable from 1 to 29.9 pps in 0.1-pps steps. Percent break is adjustable from 10 to 89.9 percent in 0.1-percent steps. And interdigit times from 10 to 990 milliseconds can be selected in 10-millisecond increments.

1.20 Selected speed and percent break values apply to all outpulsing . . . whether continuous pulsing or dialed digits. Selectable leak impedance networks (A, B, C, D, D1, SF1) and loop resistance (0 to 6300 Ω, 100-Ω steps) can also be imposed on outpulsing in loop modes.

1.21 RECEIVE SECTION

1.22 The speed measurement of received pulsing has an accuracy of ±0.1 pps over a range from 4 to 29.9 pps. The percent break of received pulsing is measured with an accuracy of ±0.5 percent over a range of 10 to 89.9 percent. Interdigit time is measured over a range of 250 to 999 milliseconds with an accuracy of ±1 millisecond.

1.23 With continuous pulsing as the input, the average pulsing speed and percent break is automatically updated and displayed after each group of 10 pulses is received. When dialed digits are being measured, the average pulsing speed and percent break parameters are updated after each non-one digit is received. Pulsing speed and percent break data is not available for dialed digits having a value of 1.

1.24 Besides average pulsing speed and percent break, other measurement data is accumulated and displayed by the instrument as mentioned previously in paragraph 1.4. Any parameter can be measured on a bridging or terminated basis.

1.25 MECHANICAL

1.26 The Model 1260A is housed in a combination portable and rack-mount case. Rugged construction enables the instrument to stand up under hard-use conditions. Included as standard equipment are:

- ☐ A carrying handle for portable use;
- ☐ A tilt stand for table top operation; and
- ☐ Brackets for mounting in 19-inch or 23-inch racks.

1.27 INPUT POWER (DC)

1.28 The 1260A operates from 48 V dc office battery at one ampere maximum. Input power can be applied via either a type 310 jack or a rear panel barrier strip. The type 310 jack is generally the most convenient connector for portable operation, while the barrier strip is generally the most convenient connector for rack-mount operation.

1.29 AC POWER OPTION

1.30 An ac power option is available to permit operation from 115/230 V ac, 50 to 60-Hz power. The option is factory installed when ordered concurrently with the 1260A. Alternatively, the option can be purchased separately at any time for field installation in a standard 1260A.

1.31 SF ADAPTER OPTION

1.32 The optional send/receive SF module gives 2600-Hz SF signaling capability to the basic Model 1260A. It plugs into a slot located in the left portion of the instrument's front panel.

1.33 The SF module provides SF send levels and receive sensitivities appropriate for the line or drop direction of the test (i.e. they conform to standard four-wire circuit TLP levels as shown in Table 4—6). In addition, a panel control permits deviation from the fixed send levels of Table 4—6 over an 18-dB range. This capability is useful for margin testing and applications where non-standard send levels are employed.

1.34 As shown in Table 2—3, the SF module sends and measures SF pulsing over a wide range and with high accuracy. Measurements can be made on a terminated basis or under in-service conditions by bridging the line. An indicator lamp is included to show idle/busy status.

1.35 Where required, the SF module can be internally set to send 2400-Hz SF signaling. In addition, an external oscillator jack permits use of external SF sources The ability to receive SF tones other than 2600 Hz is also internally selectable.

1.36 LOCAL PULSE REPEATING ARTLINE OPTION

1.37 The optional artline module allows balanced loop resistance to be placed in series with the tip and ring of the LOOP RCV jack when receiving either dry loop or wet loop pulsing. A flashing indicator serves as a reminder when any amount of loop resistance has been selected . A through mode allows the module to be bypassed when desired.

1.38 MONITOR ADAPTER OPTION

1.39 The optional monitor adapter module allows the operator of the 1260A to establish a communications line to a fellow craftsman when coordinated testing is required. It also allows the 1260A to be used as the pulsing source to set up this communications link.

SECTION 2

SPECIFICATIONS

2.1 Tables 2–1 through 2–4 list specifications for the standard Model 1260A Pulsing Test Set, the ac power option, the SF Adapter option, and the Local Pulse Repeating Artline option.

Table 2–1. Model 1260A Pulsing Test Set Specifications.

SEND SECTION	
Speed	
Range	1.0 to 29.9 pps
Resolution	0.1 pps
Accuracy	±0.1 pps
Percent Break	
Range	10 to 89.9% break
Resolution	0.1% break
Accuracy (Wet Loop)	±1.0% break
Accuracy (All other modes)	±0.5% break
Interdigit Time	
Range	10 to 990 msec
Resolution	10.0 msec
Accuracy	±1.0 msec
Loop Resistance	
Range	0 to 6.3 kΩ
Resolution	100 Ω
Accuracy	±1.5%
Line Leak Networks	Standard types A, B, C, D, D1, and SF1
Pulsing Relay	Mercury-wetted, contacts internally fused at 1 ampere
Outpulsing	
Continuous	Continuous outpulsing at speed and percent break set on thumbwheels
Keypad	Outpulsing of selected digits (0 through 9) at speed, percent break, and interdigit time set on thumbwheels
Memory	Outpulsing of stored digit sequence up to 16 digits long at speed, percent break, and interdigit time set on thumbwheels
RECEIVE SECTION	
Speed	
Range	4 to 29.9 pps
Accuracy	±0.1 pps*
	NOTE
	Pulsing speed restricts the percent break range.

*Not measured in A-relay terminated or Loop bridging modes

Table 2—1. (Cont'd).

Percent Break	
Range	10 to 89.9% break
Accuracy	±0.5% break*
	NOTE
	Pulsing speed restricts the percent break range.
Speed, Percent Break Measurement Technique	
Dialed Digit Input	Speed and percent break averaged over pulses in last non-one digit received
Continuous Pulsing Input	Speed and percent break averaged over last group of 10 pulses received
Interdigit Time	
Range	250 to 999 msec
Accuracy	±1.0 msec
Over-Range Indication	Flashing "999" in ID time display
Pulse Count	
Range	1 to 999 pulses
Over-Range Indication	Flashing "999" in pulse count display
Digit Memory	
Capacity	16 digits
Display Method	Recall and display of one digit at a time starting with first digit received
Input Impedance	
Bridge or Monitor	> 20 kΩ for both Loop and E&M
Termination	400 Ω for Loop; approximately 1.5 kΩ in series with zener diode for E&M
A-Relay	Type 221A incoming selector relay
POWER INPUT	
CO Battery	−42 to −56 V dc at 1 ampere maximum
AC Power Option	Nominal 115/230 V ac at 50 watts
OPERATING ENVIRONMENT	
Temperature	0° to 50°C (32° to 122°F)
Relative Humidity	0 to 75% non-condensing
DIMENSIONS	17 in w × 7½ in h × 13 in d (43.2 cm w × 19.1 cm h × 33.0 cm d) (Adapters supplied for mounting in 19-inch or 23-inch racks)
WEIGHT	14.0 lbs (6.4 kg)

*Not measured in A-relay terminated or loop bridging modes

Table 2—2. AC Power Option Specifications.

Voltage	115 or 230 V ac ± 10%
Frequency	50 to 60 Hz ± 3 Hz
Current	0.5 ampere
Power	Approximately 50 watts

Table 2—3. SF Adapter Option Specifications.

SEND SECTION	
Speed	
Range	4.0 to 14.0 pps
Accuracy	±0.2 pps
Percent Break	
Range	10.0 to 89.9% break
Accuracy	±0.5% break
Interdigit Time	
Range	250 to 990 msec
Accuracy	±1.0 msec
Frequency	2600 Hz ± 15 Hz, (internal switch allows selection of 2400 Hz)
Fixed Levels (dBm 600 ohms)	
Toward Line, On-Hook	−36 dBm
Toward Line, Pulsing	−24 dBm
Toward Drop, On-Hook	−13 dBm
Toward Drop, Pulsing	−1 dBm
Level Control	1 to 7 dB above fixed level in 2-dB steps 1 to 11 dB below fixed level in 1-dB steps
Level Accuracy	±1 dB
Source Impedance	600 Ω balanced
Distortion	< 1.5% THD
Balance	> 50 dB at 2600 Hz
DC Blocking	150 V dc maximum
Return Loss	> 21 dB (200 to 3500 Hz)
RECEIVE SECTION	
Speed	
Range	4 to 14 pps
Accuracy	±0.1 pps

Table 2—3. (Cont'd).

Percent Break	
Total Range	10 to 89.9% break
Total Range Accuracy	±2.0% break
Normal Measurement Range	50 to 75% break
Normal Measurement Range Accuracy	±1.0% break
	NOTE
	Pulsing speed restricts the percent break range.
Interdigit Time	
Range	250 to 999 msec
Accuracy	±1.0 msec
Bandwidth	Must operate 2600 Hz ± 30 Hz Must not operate 2600 Hz ± 100 Hz (Internal switch permits selection of nominal 1.5 to 4-kHz bandpass)
Dynamic Range (ref. 600 Ω)	
Pulsing	+8 to −26 dBm
Steady Tone (On-Hook)	+8 to −38 dBm
	NOTE
	Sensitivity depends on direction of test.
Termination Impedance	
Line or Drop	600 Ω balanced
Monitor	> 50 kΩ
Maximum Allowable 3-kHz Noise At Input	40 dB below TLP
Balance	> 50 dB at 2600 Hz
DC Blocking	150 V dc maximum
Return Loss	> 21 dB (200 to 3500 Hz)
Receiving Indicator	LED lamp (lighted when greater than minimum receiver level is present at RCV jack)

Table 2—4. Local Pulse Repeating Artline Option Specifications.

Loop Resistance Range	50 to 6350 ohms in 50-ohm steps
Resistance Accuracy	± 5%
Maximum Input Voltage	

SECTION 3

CONTROLS, INDICATORS, AND JACKS

3.1 This section contains a description of the controls, indicators, and jacks listed in Tables 3–1 through 3–5 and shown on Figures 3–1 and 3–2.

Table 3–1. Model 1260A Controls, Indicators, and Jacks

REFERENCE DESIGNATOR	CONTROL, INDICATOR OR JACK	FUNCTION
	POWER SECTION	
J6	CO BATT jack (side panel)	Type 310 jack for connection of central office battery input power (T = −48 V, S = ground). Generally the most convenient dc power connector for portable operation.
TB1	−48 V terminal strip (back panel)	Screw terminal connections for central office battery input power. (Unmarked terminals are not used.) Generally the most convenient dc power connector for rack-mount operation.
J5	GND jack	Provides a CO ground reference connection for Model 1260A.
S1	POWER ON-OFF switch/indicator/2.5 ampere circuit breaker	When set to ON position, −48 V applied to unit and red indicator lights. When circuit breaker tripped, switch set to OFF position. When placed at ON position, breaker resets.
	SEND SECTION	
S20	SEND mode switch	Selects one of several loop, E&M, or SF send modes.
S21	ON HOOK/ OFF HOOK + DIAL/ CONT switch	Controls the on-hook/off-hook pulsing status of the send port selected by the SEND mode switch. ON HOOK position sends a continuous on-hook signal. OFF HK + DIAL position sends a continuous off-hook signal until digits are dialed via keypad. Entered digits are outpulsed at selected speed, percent break and interdigit time. Upon completion of outpulsing, send port returns to steady off-hook. CONT position sends continuous stream of pulses at selected speed and percent break.
DS4	SEND monitor lamp	Follows supervision and pulsing sent by 1260A: ☐ Lights during steady on-hook periods, ☐ Is dark during steady off-hook periods, and ☐ Flashes during outpulsing.

Table 3—1. (Cont'd).

REFERENCE DESIGNATOR	CONTROL, INDICATOR OR JACK	FUNCTION
S23, S24, S25	SEND PPS thumbwheels	Set outpulsing speed from 1.0 to 29.9 pulses per second in 0.1-pps increments.
S26, S27, S28	SEND % BREAK thumbwheels	Set percent break for all outpulsing from 10.0 to 89.9 percent break in 0.1-percent increments.
S29, S30	SEND ID × 10 MSEC thumbwheels	When dialing from memory, these thumbwheels set the interdigit time from 10 to 990 milliseconds in 10-millisecond increments. When dialing in the immediate-dial mode, the ID thumbwheels determine the interdigit time only if each digit is entered prior to completion of outpulsing of preceding digit. Otherwise, the interdigit time is determined by the rate of digit entry.
S17	Dial Keypad	Provides for entry of digits to be dialed. Digits can be dialed immediately as entered, or stored for dialing from memory when desired.
DS5	STORE DIGITS monitor lamp	Lights to indicate dialing digits are stored in memory. Flashes to indicate memory is ready to accept digits. Darkens when memory is cleared.
S5 through S10	LOOP RES switches	Select loop resistances to be placed in series with the line under test during loop outpulsing. Switches can be used in combination to select loop resistances from 100 to 6300 ohms in 100-ohm increments. Releasing all LOOP RES switches selects a resistance of zero ohms.
S11 through S16	LINE LEAK switches	Select leak impedance to be shunted across the line during loop outpulsing. Standard A, B, C, D, D1, and SF1 values are available.
RECEIVE SECTION		
S19	RECEIVE mode switch	Selects one of several loop, E&M, or SF receive modes.
S18	E&M/LOOP key switch	Selects the termination/receive impedance for loop and E&M pulsing measurements. Also controls the E&M send/receive configuration. When a loop receive mode is selected (RECEIVE mode switch S19 set to either DRY LOOP or WET LOOP) the E&M/LOOP key switch provides the following functions: ☐ TERM position selects a 400-ohm resistive termination for loop pulsing measurements. ☐ BRDG WET position selects a bridging impedance exceeding 20 kohms for measurements on wet loops only.

Table 3—1. (Cont'd).

REFERENCE DESIGNATOR	CONTROL, INDICATOR OR JACK	FUNCTION
S18 (Cont'd).	E&M/LOOP key switch (Cont'd).	☐ A-RELAY position selects an internal A-relay termination for loop pulsing measurements. The A-relay coil terminates the line under test, while measurements are made across the relay's contacts. When any E&M send or receive mode is selected (via SEND/RECEIVE mode switches) the E&M/LOOP key switch provides the following functions: ☐ Either SEND-RCV position selects for the desired E&M pulsing measurement a low impedance termination that approximates the normal in-service termination. In addition, the 1260A's E&M jacks are configured for sending as well as receiving toward line or drop. Two identical SEND-RCV positions are provided for flexibility in mixed loop and E&M operating modes. For example, when sending on E lead toward drop while receiving on loop basis, top position allows selection of 400-ohm termination for loop; bottom position allows selection of A-relay termination for loop. Either position permits sending on E lead. ☐ THRU & MON position selects a bridging impedance exceeding 20 kohms for the desired E&M measurement. E&M jacks are through-connected (connected in parallel). This position inhibits sending on an E&M basis.
S3	MAX pushbutton	When pressed and held, selects display of maximum (highest) pulsing speed and percent break measured since last reset.
S4	MIN pushbutton	When pressed and held, selects display of minimum (lowest) pulsing speed and percent break measured since last reset.

NOTES

1. The speed and percent break values displayed concurrently when either the MAX or MIN pushbutton is pressed are not necessarily associated with the same pulse period.

2. Engaging both the MAX and MIN pushbuttons simultaneously resets the receive section. The display is cleared along with all stored measurement data.

Table 3—1. (Cont'd).

REFERENCE DESIGNATOR	CONTROL, INDICATOR OR JACK	FUNCTION
S2	COUNT-ID-DIGITS pushbutton	Provides the following display functions: ☐ When released permits display of average received pulsing speed and percent break. ☐ When pressed and held, selects a display of total count of all pulses received since last reset, plus a display of minimum (shortest) interdigit time measured. ☐ When alternately released and re-engaged (within two seconds of release) provides a means of selecting for display an individual dialed digit from among up to 16 digits received. Displayed with each digit is the interdigit time following that digit. In addition, each displayed digit is identified as to its position (from 1 to 16) in the received digit sequence.
U1 through U6	PPS-PULSE COUNT-DIGIT and % BREAK-ID readouts	Six-digit display for selective viewing of the data accumulated by the 1260A receive section.
M1	Meter	Provides an analog indication of percent break and on-hook/off-hook status in all receive modes.
R2	METER ADJ potentiometer	Allows meter percent break indication to be set to agree with digital readout.
INPUT/OUTPUT JACKS AND MONITOR INDICATORS		
J1	LOOP SEND 310 jack	Output port for loop pulsing.
J2	LOOP RCV 310 jack	Input port for loop pulsing.
J3	E&M LINE 310 jack	Provides a means for sending on the M lead towards line and receiving on the E lead from line.
J4	E&M DROP 310 jack	Provides a means for sending on the E lead towards the drop and receiving on the M lead from the drop.
DS3	SLEEVE GND monitor lamp	Sleeve lead idle/busy indicator. Lights to indicate busy (presence of ground on sleeve of LOOP RCV jack).
DS1	E monitor lamp	E lead idle/busy indicator. Lights to indicate idle (absence of ground on tip of E&M LINE jack). Flashes while receiving E lead pulsing.
DS2	M monitor lamp	M lead idle/busy indicator. Lights to indicate idle (absence of battery on ring of E&M DROP jack). Flashes while receiving M lead pulsing.

Table 3—1. (Cont'd).

REFERENCE DESIGNATOR	CONTROL, INDICATOR OR JACK	FUNCTION
	INTERNAL SWITCHES	
S22	E-Suppression circuit toggle switch	Provides a means of switching a 0.15-uF, 330-ohm suppression network across the 1260A's E lead pulsing contacts. This network emulates the actual pulsing suppressors found on many E lead pulsing receivers. Factory setting switches the suppression network out.
A6S1	Input pulse timer micro DIP switch	Determines the amount of transient/noise immunity possessed by the 1260A's receive section. Can be set to ignore transients less than 6.4, 12.8 or 25.6 milliseconds. Switch is set to 12.8-millisecond position at the factory.

Table 3—2. Ac Power Option Controls, Jacks, and Fuses.

REFERENCE DESIGNATOR	CONTROL, JACK OR FUSE	FUNCTION
J1	AC jack (rear panel)	Receptacle for ac power cord supplied with option. Can accept either 115 V or 230 V, 50 to 60-Hz power.
S1	115/230 slide switch	Selects operation from either 115 V or 230 V ac power.
F1/F2	AC line fuses	Provides 2 ampere overcurrent protection for the ac input line. One fuse protects each side of the line.
		WARNING **Disconnect power cord before checking fuses.**

Table 3—3. SF Adapter Option 1260-10 Controls, Indicators, and Jacks.

REFERENCE DESIGNATOR	CONTROL, INDICATOR OR JACK	FUNCTION
S3	DEV FR SND TLP rotary switch	Provides the capability of sending SF signaling above and below the module's fixed send levels. Levels up to 7 dB above fixed send levels can be selected in 2-dB steps. Levels as low as 11 dB below fixed send levels can be selected in 1-dB steps.
S2	SEND-RCV LINE/MON/ SEND-RCV DROP switch	Configures the SF module for bridging/monitoring line under test, or for send/receive testing towards line or drop. ☐ The SEND-RCV LINE position sets the appropriate transmitter send levels and receiver sensitivities for send/receive testing towards the line. Also, the receiver is terminated in 600 ohms.

Table 3—3. (Cont'd).

REFERENCE DESIGNATOR	CONTROL, INDICATOR OR JACK	FUNCTION
S2 (Cont'd).	SEND-RCV LINE/MON/ SEND-RCV DROP switch (Cont'd).	☐ The SEND-RCV DROP position sets the appropriate transmitter send levels and receiver sensitivities for send/receive testing towards the drop. The receiver is terminated in 600 ohms. ☐ The MON position enables monitoring of in-service SF circuits and high impedance (50 kohms) bridging measurements. A through-connection is established from the SF RCV jack to the SF SEND jack while the latter jack is isolated from the transmitter.
J1	EXT OSC 310 jack	Allows use of an external SF source for SF send testing. The internal SF source is automatically disabled when this jack is in use.
J2	SF SEND 310 jack	Module's SF output port.
J3	SF RCV 310 jack	Module's SF input port.
DS1	CKT IDLE monitor lamp	SF supervision indicator. Lights to indicate presence of SF tone (idle condition) at SF RCV jack. Flashes when SF pulsing is received.
S1	Internal DIP multiple switch	Allows selection of the following: ☐ 2400 or 2600-Hz SF send frequency. (The latter is the normal selection.) ☐ Wideband (1.5 to 4 kHz) or narrow band (2600 ± 30 Hz) SF receiver. (The latter is the normal selection.) ☐ Send level augmentation.

Table 3—4. Local Pulse Repeating Artline Option 1260-12 Controls and Indicators.

REFERENCE DESIGNATOR	CONTROL OR INDICATOR	FUNCTION
DS1	LINE RESISTANCE indicator	When flashing, indicates that some resistance has been inserted between the LOOP RCV jack and the receiver function on the 1260A.
S1H	THRU pushbutton	When pressed and latched, bypasses the Artline.
S1A through S1G	50, 100, 200, 400, 800, 1600, and 3200 pushbuttons	When any is pressed and latched, places the indicated loop resistance between the LOOP RCV jack and the receiver function on the 1260A. One half of the selected resistance is placed in each of the tip and ring leads. Any or all can be selected simultaneously for a range of 50 to 6350 ohms.

Table 3–5. Monitor Adapter Option 1260-13 Controls and Jacks.

REFERENCE DESIGNATOR	CONTROL OR JACK	FUNCTION
J1	MONITOR jack	310 jack for headset to monitor line connected to J2 when S1 is in MONITOR position.
J2	SEND LOOP jack	310 jack to send pulsing provided by 1260A when S1 is in SEND LOOP position or to talk over when S1 is in MONITOR position.
S1	MONITOR/SEND LOOP switch	When in SEND LOOP position, connects SEND LOOP jack to SEND LOOP jack on 1260A. When in MONITOR position, connects MONITOR jack to SEND LOOP jack and opens connections to 1260A.

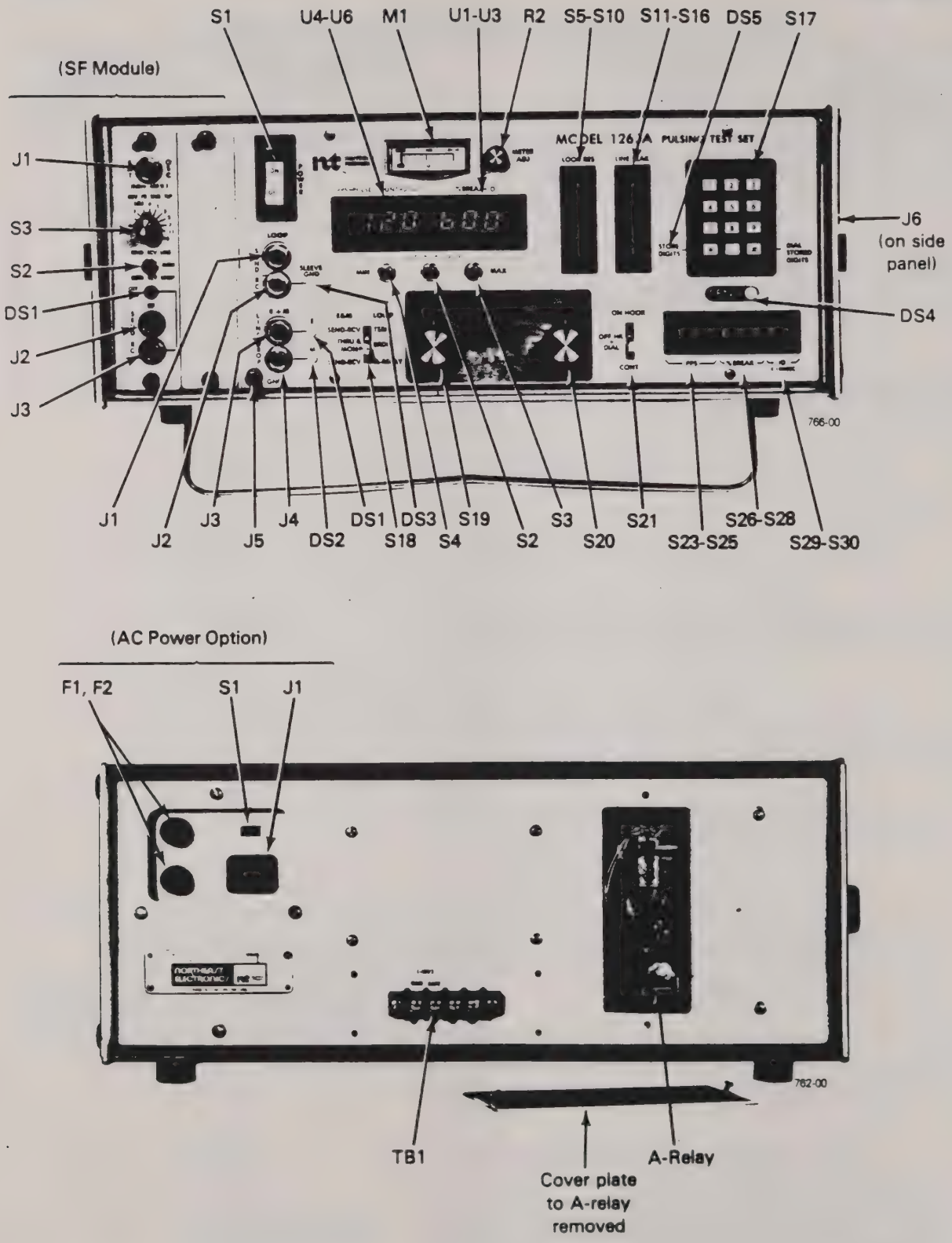


Figure 3—1. Model 1260A and SF Adapter Option 1260-10 Controls, Indicators, and Jacks.

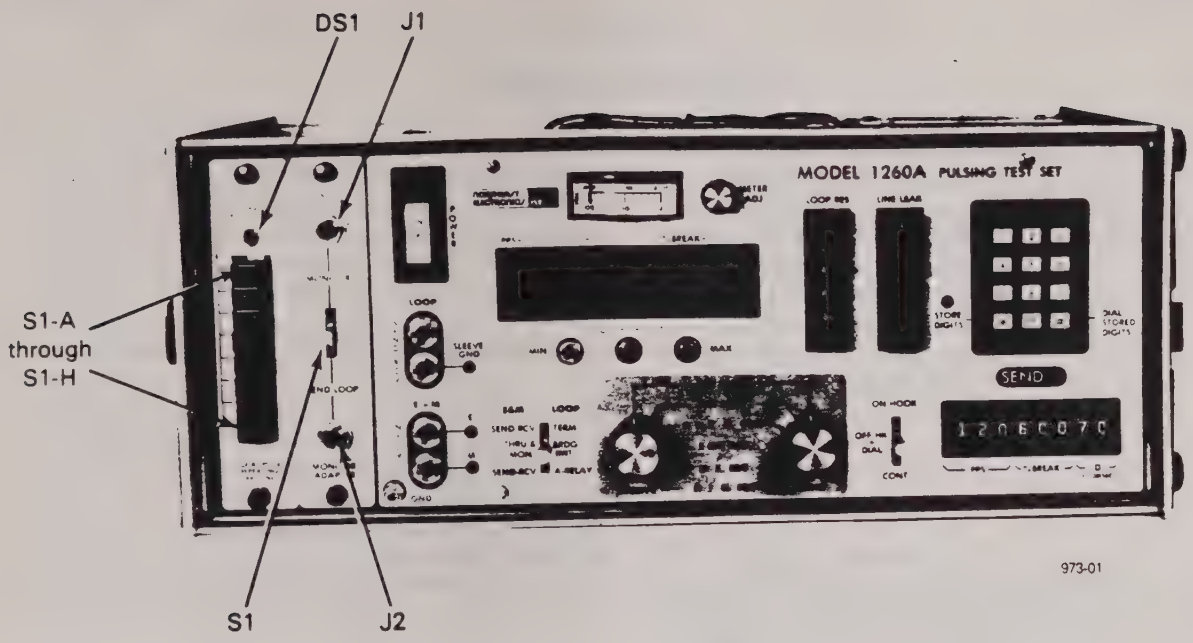
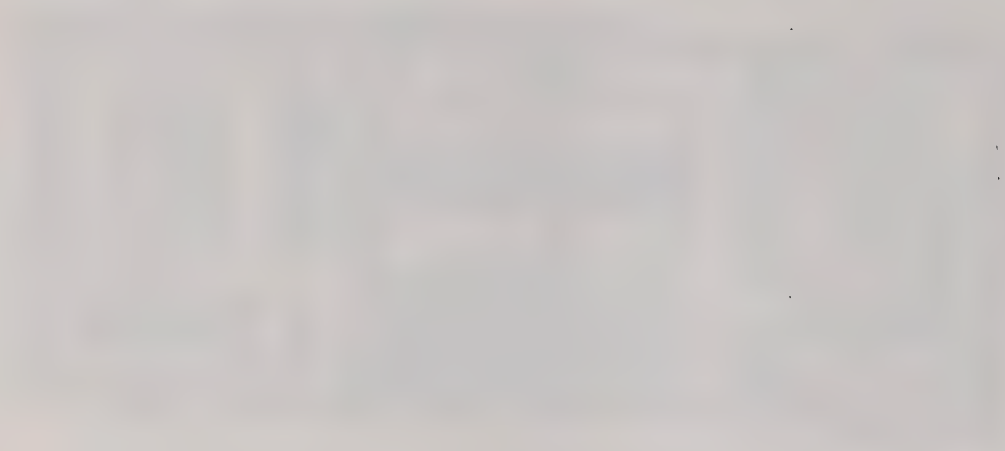
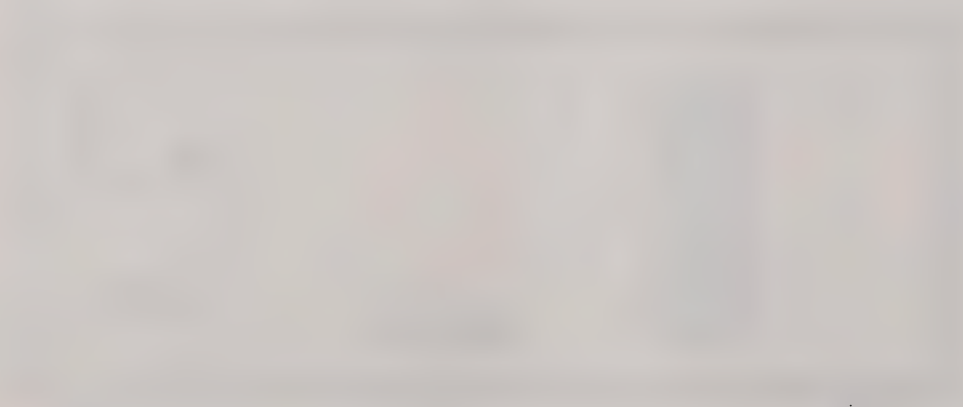


Figure 3—2. Local Pulse Repeating Artline Option 1260-12 and Monitor Adapter Option 1260-13 Controls, Indicators, and Jacks.





SECTION 4

THEORY OF OPERATION

4.1 This section provides circuit descriptions for the Model 1260A Pulsing Test Set and available options. Being a microprocessor-directed instrument, the 1260A has very definite functional sections. A detailed circuit description of each functional section is presented following an introductory overall block diagram description.

4.2 OVERALL BLOCK DIAGRAM DESCRIPTION

4.3 As shown on Figure 4—1, the 1260A is comprised of 11 functional sections. These are: (1) switch status; (2) dial keypad entry; (3) transmitter; (4) monitor; (5) receiver; (6) interrupt and display; (7) CPU; (8) power supply and distribution; (9) ac power option; (10) SF Adapter option; and (11) Local Pulse Repeating Artline option. Except for the monitor, power supply, and all options, all functional sections share the use of the CPU.

4.4 All of the sections except monitor, power supply, and all options operate on an I/O port basis. Data is transferred over the data bus from the CPU to the I/O ports and vice versa. Control of data transfer at the ports is a function of certain memory addresses appearing on the address bus as well as control instructions appearing on the control bus. CPU operation is controlled by the program permanently stored in a portion of memory.

4.5 The dial keypad entry function and part of the switch status function exercise indirect control over the transmitter. The switch status function monitors the position of the ON HOOK/OFF HK-DIAL/CONT switch and the PPS, % BREAK, and ID thumbwheel switches to control these parameters as they affect the transmitter. The dial keypad entry function determines the digits to be transmitted when the ON HOOK/OFF HK-DIAL/CONT switch is in the OFF HK-DIAL position. In addition, it selects the store digits mode and initiates automatic dialing of the digits stored. An LED indicates when it is permissible to enter and store digits. The SEND mode switch and the LOOP RES and LINE LEAK pushbuttons all affect the output line conditioning circuits of the transmitter, and as such, are not under software control. The SEND indicator follows on-hook/off-hook supervision and pulsing. Part of the E&M/LOOP switch provides some necessary signal routing. The transmitter output is applied to either the LOOP SEND, E&M LINE, or the E&M DROP jack as controlled by the SEND mode switch. If the SF Adapter option is installed, the transmitter pulses are also applied to this option for conversion to SF.

4.6 The signals present at the E&M LINE, E&M DROP, and the LOOP RCV jacks are the receiver inputs. The RECEIVE mode switch controls the input selection. If the Local Pulse Repeating Artline option is installed, loop resistance can be inserted ahead of the receiver to simulate receive line losses for dry and wet loop pulsing. An indicator serves as a reminder that loop resistance is present. The Artline can also be bypassed. Part of the E&M/LOOP switch and the RECEIVE mode switch serve only to control the receiver interface and route the signal to the appropriate circuits. If the SF Adapter is installed, this option supplies the receiver input after the SF has been converted to dc pulsing levels. The meter simply gives an analog feel by displaying the percent break and the on/off-hook supervision status.

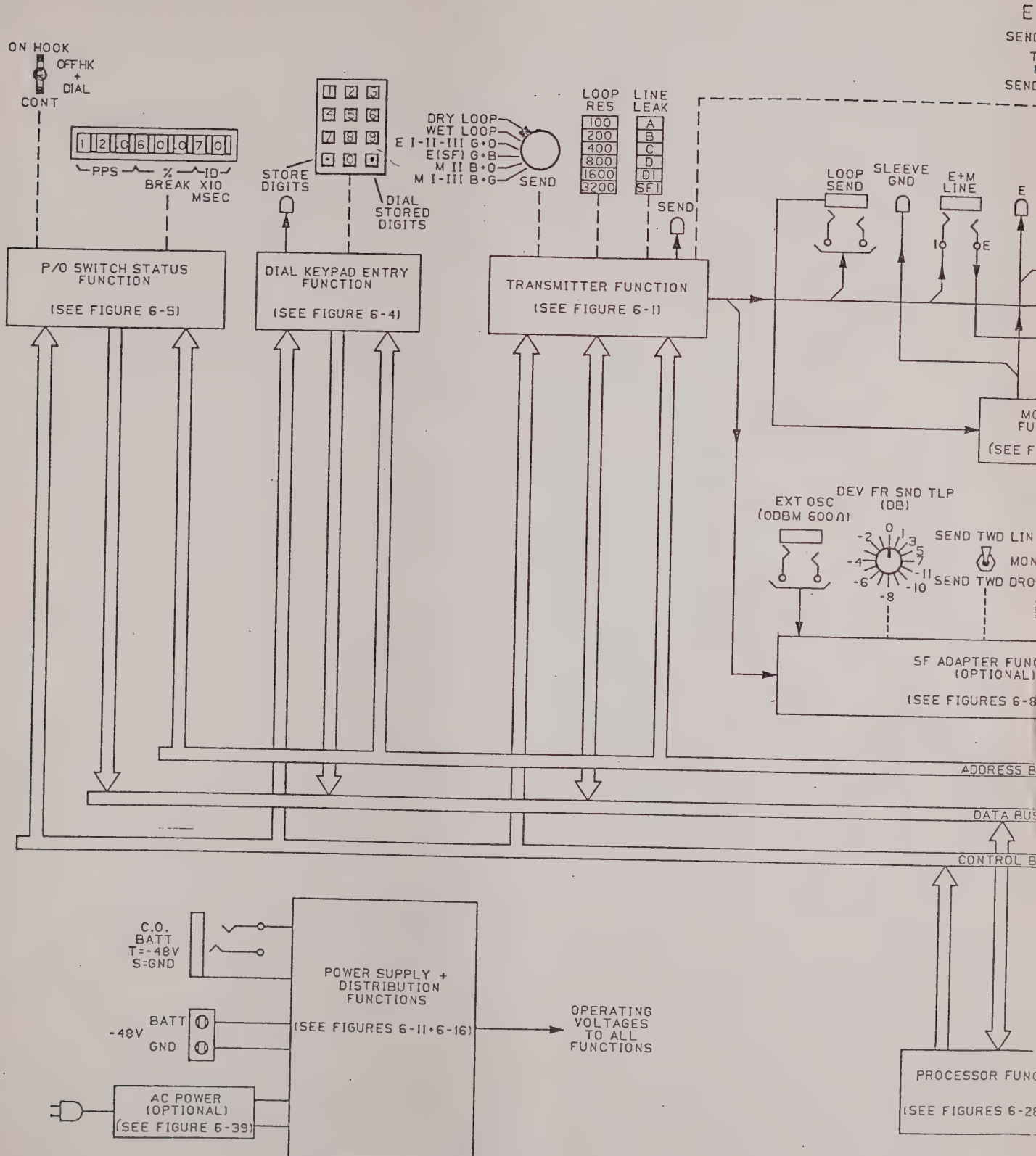
4.7 After the received signal parameters have been measured by the CPU, the digital display is periodically updated with the average pulse speed and percent break information through the interrupt and display function. The digital display also displays other parameters as controlled by the MIN, MAX, and COUNT-ID-DIGITS pushbuttons that are part of the switch status function. These parameters include the minimum and maximum pulse speed and percent break, interdigit time, total pulses counted, digits received, and the sequential position of digits in relation to the total series received.

4.8 The monitor function simply detects and displays the supervision status of the LOOP SEND jack sleeve, the E&M LINE jack E lead, and the E&M DROP jack M lead. No software control is required for this function.

4.9 The SF Adapter option provides for the sending and receiving of SF signaling. The option converts 1260A transmitter dc pulsing levels to SF levels and makes them available at the SF SEND jack. The specific levels sent are determined by a combination of the DEV FR SND TLP and the SEND-RCV LINE/MON/SEND-RCV DROP switches. The EXT OSC jack allows an external source to supply the SF tone. A CKT IDLE indicator displays the supervision status present at the SF RCV jack. SF signals appearing at the RCV jack are converted to dc pulsing levels, which are then processed by the 1260A receiver.

4.10 The heart of the unit is the CPU. It interfaces with most of the other functions via the address, data, and control buses. For the transmitter, the CPU monitors the appropriate switches and converts this information to corresponding pulse speed, percent break, interdigit time, and digit information. Similarly, the CPU operates on the received pulse data, calculates, and displays the pulse speed, percent break, interdigit time, and dialed digit information.

4.11 Central Office battery of – 48 V dc can be used to power the unit via a 310 jack or a terminal strip. When the ac power option is installed, conventional ac power can be used. In either case, – 48 V dc is applied to the power supply and distribution system to generate the several operating potentials required by the unit.


ON HOOK
OFF HK + DIAL
CONT
PPS
% BREAK
ID XIO MSEC
STORE DIGITS
DIAL STORED DIGITS
DRY LOOP
WET LOOP
E I-II-III G+O
E(SF) G+B
M II B+O
M I-III B+G
SEND
LOOP RES
LINE LEAK
100
200
400
800
1600
3200
A
B
C
D
D1
SF1
SEND
LOOP SEND
SLEEVE GND
E+M LINE
P/O SWITCH STATUS FUNCTION
(SEE FIGURE 6-5)
DIAL KEYPAD ENTRY FUNCTION
(SEE FIGURE 6-4)
TRANSMITTER FUNCTION
(SEE FIGURE 6-1)
EXT OSC (0DBM 600Ω)
DEV FR SND TLP (DB)
SEND TWD LIN
SEND TWD DRO
SF ADAPTER FUNC (OPTIONAL)
(SEE FIGURES 6-8
ADDRESS B
DATA BUS
CONTROL B
C.O. BATT T=-48V S=GND
-48V
BATT
GND
POWER SUPPLY + DISTRIBUTION FUNCTIONS
(SEE FIGURES 6-11+6-16)
OPERATING VOLTAGES TO ALL FUNCTIONS
AC POWER (OPTIONAL)
(SEE FIGURE 6-39)
PROCESSOR FUNC
(SEE FIGURES 6-2

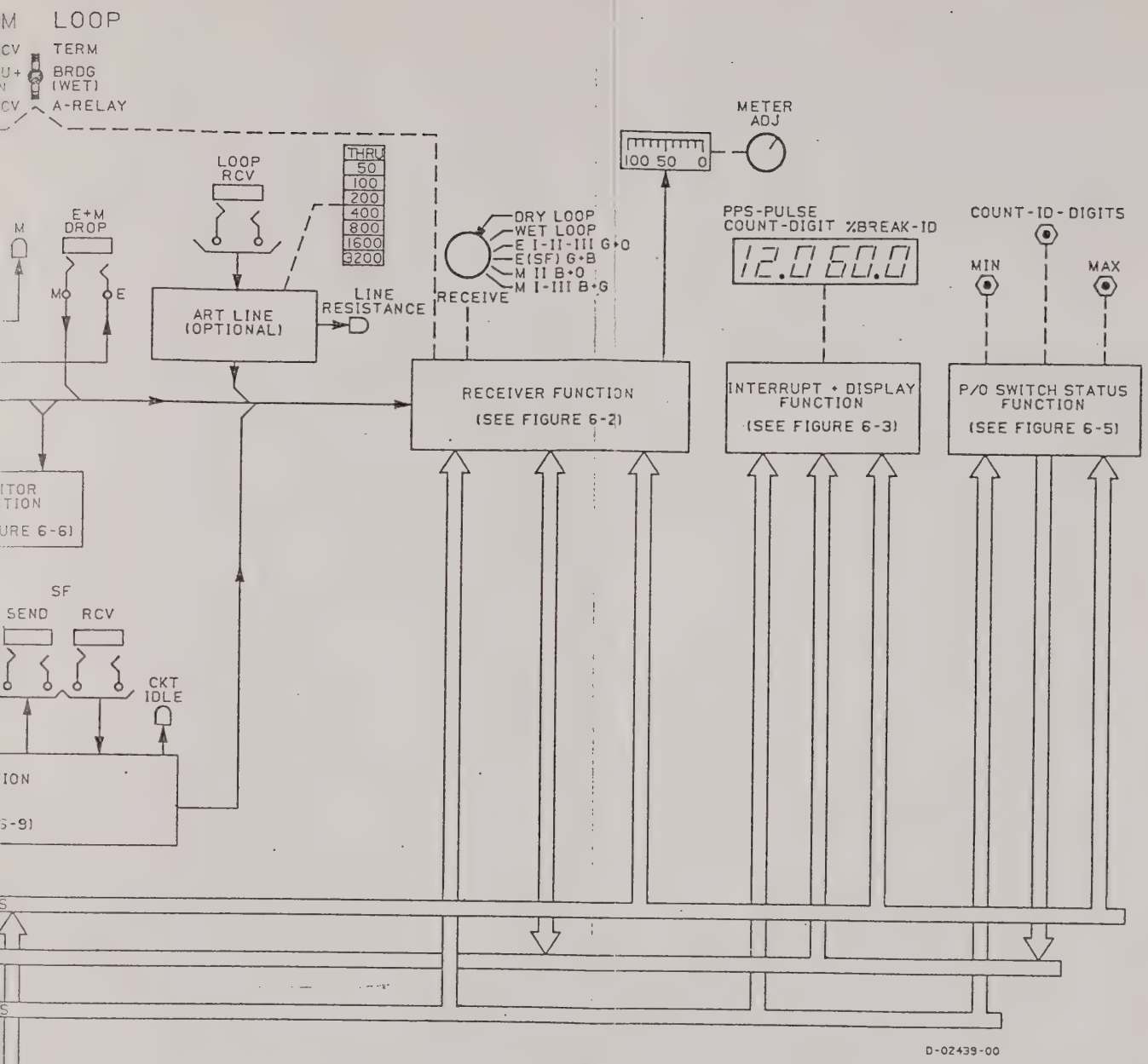


Figure 4—1. Model 1260A Overall Functional Block Diagram.

4.12 TRANSMITTER BLOCK DIAGRAM DESCRIPTION

4.13 Figure 4—2 shows a simplified block diagram of the transmitter. The purpose of the transmitter is to generate dialed digits or continuous pulses at the speed, percent break, and interdigit time specified by the SEND controls. The CPU converts the pulsing speed and percent break information it obtains from the front panel switches into digital words that are applied to the data bus. These words are latched and used to preset the counter. Decoded memory addresses control the movement of data within the transmitter. The number preset into the counter is the difference between the maximum count that the counter is capable of and the desired count. In this manner the number of pulses counted until the counter overflows, multiplied by the 25-microsecond period of the 40-kHz pulses counted, represents the desired time interval.

4.14 The make and break intervals represent the pulsing speed and percent break desired. The SEND indicator follows the supervision and pulsing transmitted. The pulsing relay is the interface between the transmitter output and the circuit under test. Whether the output is sent to the loop, or the E&M jacks and the selection of the appropriate combination of battery, ground, and open are the functions of the line conditioning circuits, they are under direct control of the SEND and E&M/LOOP switches. Line leak and loop resistance can be added to the loop send function only.

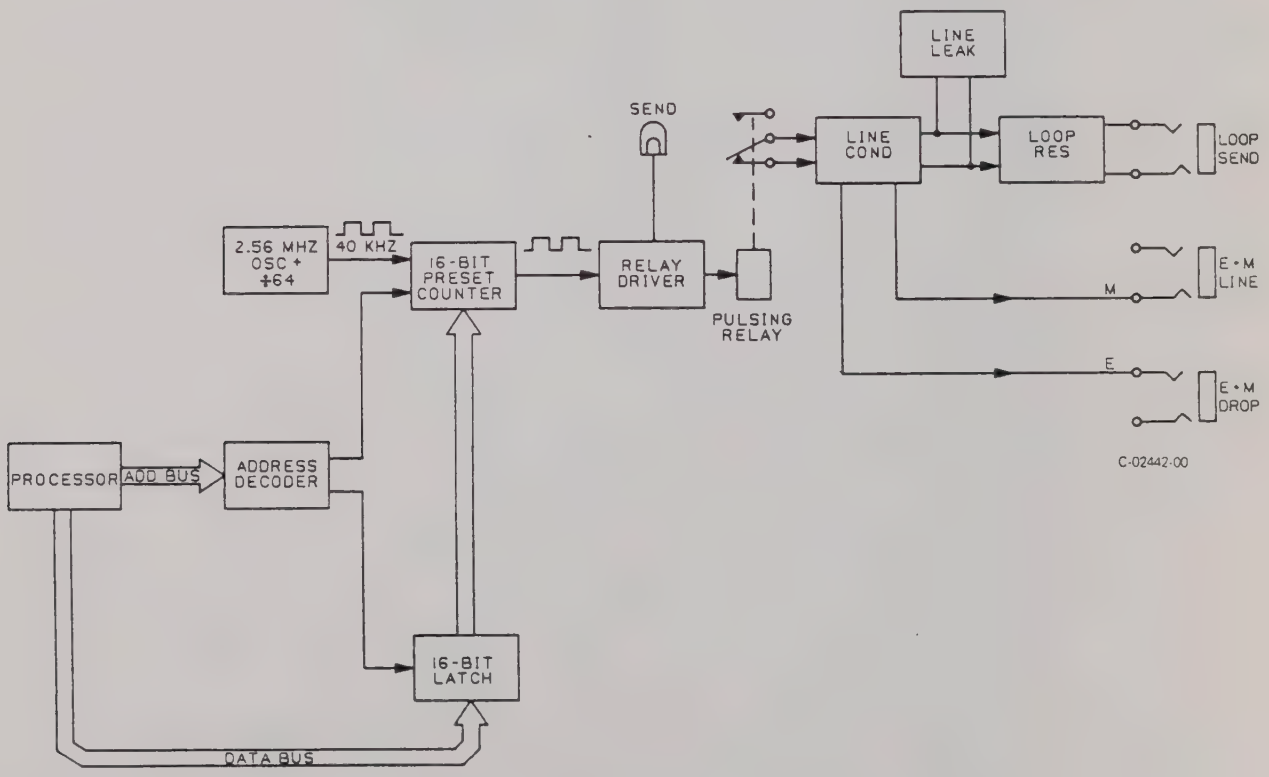


Figure 4—2. Transmitter Block Diagram.

4.15 TRANSMITTER DETAILED CIRCUIT DESCRIPTION

4.16 See Figure 6—1 for the transmitter functional schematic diagram. The portion of the transmitter shown on the left hand page is the digital section and that on the right hand page is the analog section.

4.17 DIGITAL SECTION OF THE TRANSMITTER

4.18 The main function of the digital section is to generate break and make time intervals of the desired pulsing speed and percent break as set by the front panel switches. This section consists of an address decoder, a 40-kHz generator, and a digital-to-time interval converter.

4.19 Address Decoder

4.20 The address decoder utilizes certain memory address locations placed on the address bus by the software to control the events occurring during the digital-to-time interval conversion. Address bits A0 through A4 and A8 through A15 in conjunction with control lines HLDA, MEMR, and MEMW are used for address decoding. These are outputs of CPU U9 and system controller U7 located on A8. The HLDA output of U9 is always in the non-active or low state. This is used to permanently enable tri-state bus drivers U4, U5, and U6.

4.21 Address bits A8 through A15 are buffered by U5 and U6 and then applied to open collector AND gates U2A, U2B, and U2C. When A8 through A15 are all high the AND gate output goes high, is buffered by U4, and appears as an output line designated I/O. This corresponds to memory locations FFXXH and has been chosen to enable the I/O ports. The remaining five bits are buffered in U4 and U5 and are then designated AB0 through AB4. They form the XX part of the general FFXXH locations. The final two lines used in decoding are MEMR and MEMW that are present at the output of U7 when there is a read or write command respectively.

4.22 Address decoders U16 and U17 located on A7 are devices that have two enable inputs and three binary inputs. When the G1 enable is high and the G2A/B enable is low, the Y outputs go low one at a time in accordance with the binary inputs. Tables 4—1 and 4—2 show how these inputs are decoded to form the six read and the three write command decodes.

Table 4—1. Transmitter Read Address Decoding Truth Table.

MEMR	I/O	AB4	AB3	AB2	AB1	AB0	FF00H(R)	FF01H(R)	FF02H(R)	FF05H(R)	FF06H(R)	FF07H(R)
L	H	L	L	L	L	L	L	H	H	H	H	H
L	H	L	L	L	L	H	H	L	H	H	H	H
L	H	L	L	L	H	L	H	H	L	H	H	H
L	H	L	L	H	L	H	H	H	H	L	H	H
L	H	L	L	H	H	L	H	H	H	H	L	H
L	H	L	L	H	H	H	H	H	H	H	H	L

Table 4—2. Transmitter Write Address Decoding Truth Table.

MEMW	I/O	AB4	AB3	AB2	AB1	AB0	FF00H(W)	FF01H(W)	FF02H(W)
L	H	L	L	L	L	L	L	H	H
L	H	L	L	L	L	H	H	L	H
L	H	L	L	L	H	L	H	H	L

4.23 **40-kHz GENERATOR**

4.24 The technique of counting a known number of pulses to generate accurate time intervals by the digital-to-time interval converter requires a source of precision pulses. This is the function of the 40-kHz generator located on A6. U18 is a combination oscillator and divide-by-64 chip. Crystal Y1 allows a highly accurate 2.56-MHz signal to be generated by U18. After a division by 64, the 40-kHz output is applied to the six inverters of U17 connected in parallel. U18 is a CMOS device and U19D is TTL. The accumulative output drive capability of U17 is required to drive the input of Inverter U19D. U1B on A6 and U37B on A7 have Schmitt trigger inputs and generate the fast rise times required by the counting circuits that follow.

4.25 **Digital-To-Time Interval Converter**

4.26 The function of the digital-to-time converter is to generate the break and make time intervals from 16-bit binary words supplied by the processor. Figure 4—3 is an event sequence diagram for the transmitter digital-to-time interval converter.

4.27 The basic technique used to generate precision time intervals is counting accurate 40-kHz pulses (period of 25 microseconds). For example, the break interval for loop pulsing at 10 pps and 50% break is 50,000 microseconds. This would require counting 2,000 of the 40-kHz pulse periods.

4.28 One way this could be done would be to preset a counter to 2,000, then count down to zero. However, the 1260A uses a counter that can count only in the up direction, so a different counter presetting technique must be used.

4.29 Returning to the example of counting 2,000 40-kHz pulses, the following presetting technique is used for the counter. The counter has a 16-bit length and thus a maximum count of 65,535. To count up 2,000 counts to this number requires a decimal preset of 63,536. As a 16-bit binary word, this would be 1111 1000 0011 0000. This is a function of the processor. The counter will now count up 2,000 counts until the counter overflows, at which time the counter will be in the all zeros state.

4.30 The sequence of events shown on Figure 4—3 represents the generation of a break interval followed by a make interval. It is assumed that the transmitter is in its idle condition, as it would be after power turn-on or initialization caused by a reset. This clears U29B so that its Q output is low to inhibit the clock at U14A. Transmit flip-flop U18B is cleared and its Q output goes low (off hook).

4.31 The first interval generated is always a break interval. The sequence is started by decoding FF00H(W) and FF01H(W), which latches the 16-bit break interval preset word into U11, U5, U8, and U2. This is immediately followed by FF02H(W) that is inverted by U13D and U15B and applied to the load input of all four preset counters. This presets the counters with the 16-bit break interval present at the output of the latches. Next, FF00H(W) and FF01H(W) are repeated in order to load the preset word for the following make interval into the latches. Now all of the required data for the first pulse period has been transferred from the processor to the digital-to-time interval converter. Generation of the respective time intervals is now ready to proceed.

4.32 Transmit enable address FF00H(R) is decoded and presets U29B. The Q output enables U14A so that 40-kHz pulses are applied to the counters. The counters now count up until one or more than the maximum of 65,535 counts is reached, at which time the QD output of U3 goes low. This signals the end of the break interval. 10-microsecond one-shot U28A is triggered by the negative QD transition and the U28A Q output is used to perform two tasks simultaneously.

1. It is applied through U15B to the load input of all counters to preset them with the make interval. Note that at the end of the 10-microsecond pulse, the counters again begin to totalize the make interval and the QD output of U3 goes high.

2. It clocks U18A to set the transmit flag high. The flag clocks U18B and the Q output of the transmit flip-flop goes low to terminte the break interval. The flag is also applied to bus drive U1B.

4 33 The transmit flag is read onto the data bus by FF02H(R) to alert the CPU that is must produce the next break preset data. The flag is immediately cleared by FF06H(R) and the count continues until the counter overflows, this terminating the make interval. The process continues as long as a transmitter output is called for.

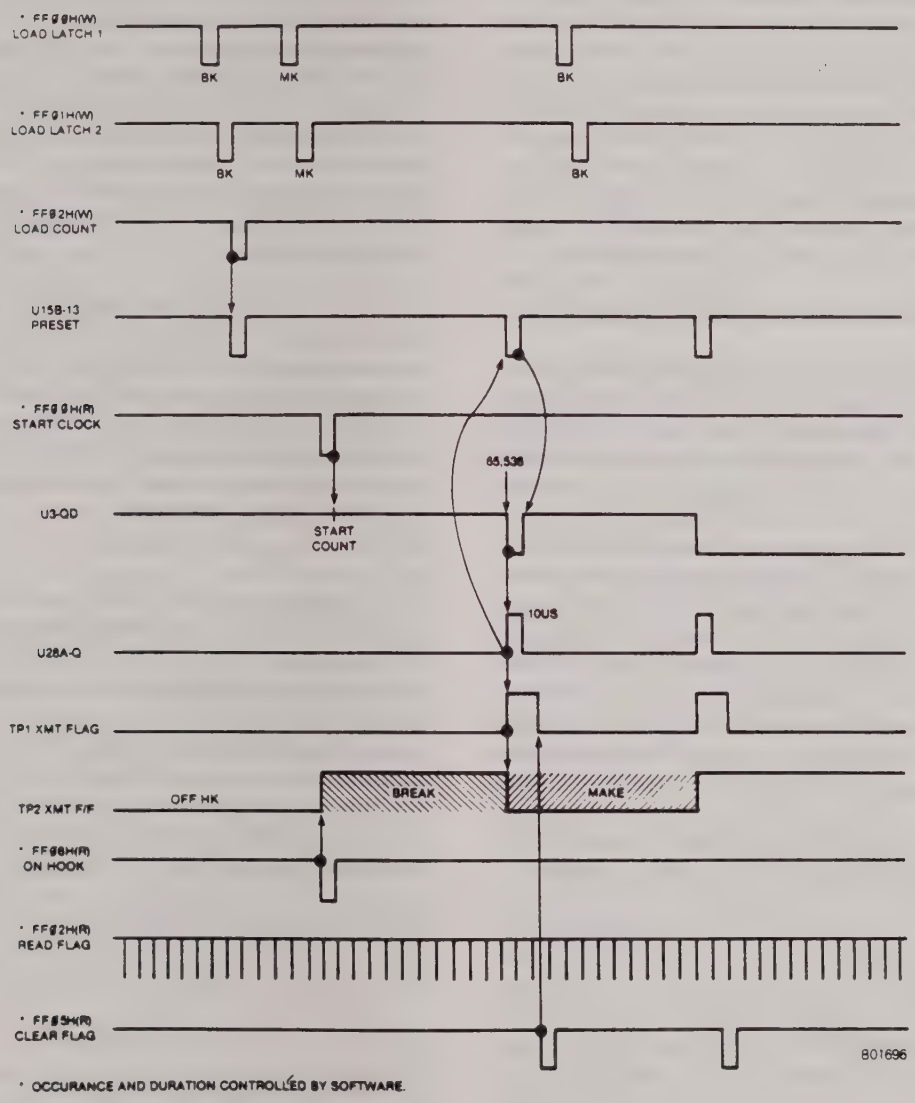


Figure 4—3. Event Sequence Diagram for the Transmitter Digital-To-Time Interval Converter.

4.34 ANALOG SECTION OF THE TRANSMITTER

4.35 The transmitter signal at the input of inverter U10D consists of make and break intervals of the proper time duration. The break interval is high at this point and the make is low. Inverter U5D provides the drive current for SEND indicator DS4 mounted on the front panel. During the break interval Q1 conducts and turns on relay driver Q2. This allows pulsing relay K1 to energize and open its contacts. The schematic shown on Figure 6—1 depicts the 1260A in the dry loop mode so that the tip and ring of LOOP SEND jack J1 are open during the break interval. Leak networks located on A4 and balanced loop resistance located on A3 are switched in as required. Switches S18 and S20 condition the K1 pulsing contacts for dry loop, wet loop, or E&M signaling.

4.36 RECEIVER BLOCK DIAGRAM DESCRIPTION

4.37 See Figure 4—4 for a simplified block diagram of the receiver. The function of the receiver is to convert the break and make time intervals present at the LOOP RCV and E&M jacks into corresponding digital words that can be used by the CPU to compute speed and percent break.

4.38 Dry and wet loop pulsing is received at the RCV LOOP jack. If the Local Pulse Repeating Artline option is installed balanced loop resistance can be placed in the receive loop, otherwise the input is routed around this function. A switch allows the use of an internal A relay termination if desired. This signal along with the inputs from either the E&M LINE or the E&M DROP jack is applied to the internal line conditioning function. This provides some mode switching and also selects the appropriate combination of battery, ground, or open to ensure that the current through input resistance R always flows in the same direction regardless of the type of pulsing being received.

4.39 The determination of whether a pulsing circuit connected to either of the input jacks is in the make or break state is accomplished by sensing current through a terminating resistance. The transition thresholds from make to break and vice versa are set by a limiter and a Schmitt trigger. A fast break detector ensures minimum pulse width distortion in the presence of capacitive contact suppression. The limiter, Schmitt trigger, and the fast break detector operate from a floating power supply. This allows a wide variation in the input voltage levels that can be detected. Power supply isolation and level transformation is provided by an opto isolator. The output level of this stage is operated from the + 5 volt supply and is compatible with the TTL logic circuits that follow. The front panel % BK meter is driven by the opto isolator output.

4.40 Any contact bounce that may be present on the received signal is still present at this point. A debouncer next removes all signal perturbations that occur within a selected time period after the first transition. A 40-kHz waveform derived from the 2.56-MHz oscillator provides the basic timing. At this point in the receiver the break/make waveform has well defined edges and is now ready to be converted to an equivalent digital word.

4.41 The basic principle of the digital conversion technique used is to count 40-kHz pulses during the time interval between edges of the input waveform. Edge detectors provide well defined transitions that are used to gate the 16-bit counter on and off. Thus the break and make intervals are represented by 16-bit words that are proportional to the time intervals. Memory adddresses furnished by the CPU are decoded and used to control the transfer of the digital information from the counter to the I/O port and then to the processor itself.

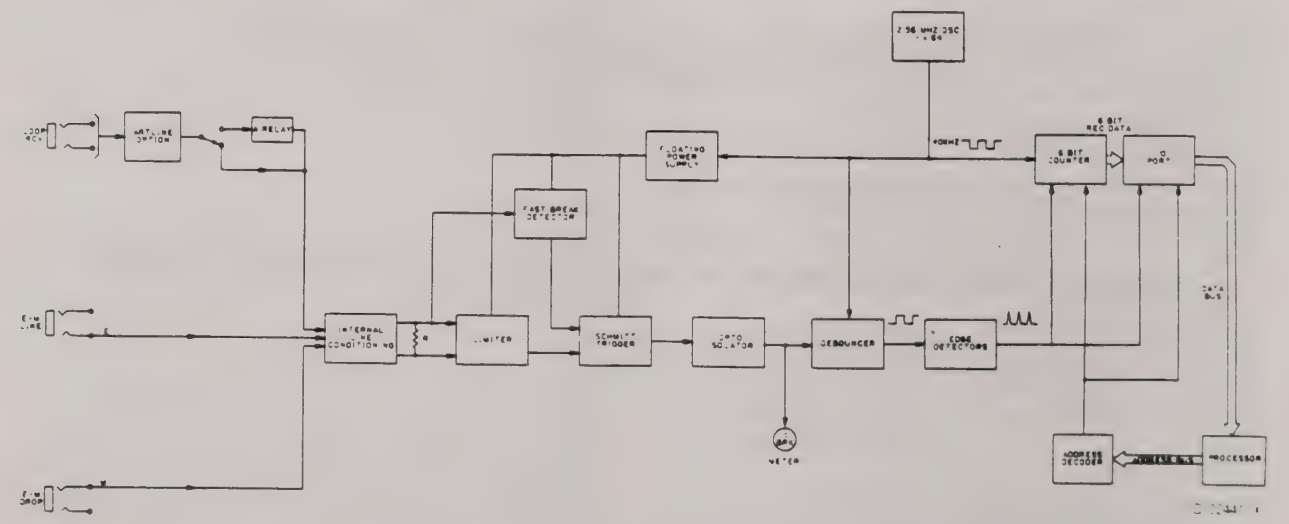


Figure 4—4. Receiver Block Diagram.

4.42 RECEIVER DETAILED CIRCUIT DESCRIPTION

4.43 See Figure 6—2 for the functional schematic diagram of the receiver. The portion of the receiver shown on the left-hand page from the input jacks to the output of the debounce circuit is the analog circuit where the signal exists in the form of break and make time intervals. The remainder of the receiver shown on the right-hand page is the digital portion where the signal exists in the form of edges, pulses, and digital words.

4.44. ANALOG SECTION OF THE RECEIVER

4.45. The functions of this section are to select the desired receive input jack, route the input signal to the appropriate functions, apply the appropriate voltages, and detect make/break transitions and generate a replica of the input that has well-defined edges.

4.46 Both dry loop and wet loop pulsing can be received at LOOP RCV jack J2. If the optional Local Pulse Repeating Artline is installed in either A14 or A15, 50 to 3200 ohms of balanced resistance can be placed in the loop under test. The input can also be carried through without any loop resistance. When no option is installed in A14 and/or A15 an installed jumper board will carry the lines through the unused slot. For both the dry loop and wet loop terminated modes, 400-ohm resistor R3 is the input resistance of the receiver. Various decks of switches S18 and S19 connect the internal battery and ground in such a manner that the R5 side of R3 is always positive with respect to the other side when current flows through it during the make (off-hook) interval. For the wet loop bridged mode, both R5 and R3 are disconnected and the receiver input resistance is that presented by assembly A6. This is the input resistance of the fast break detector as seen through the low impedance of the floating power supply. In any of the loop modes, the input pulsing can be terminated by A-relay K1 to simulate an office relay. The ground and open pulsing of the A-relay then becomes the input of the receiver.

4.47 Receiving on the E lead from the line is via E&M LINE jack J3 and receiving on the M lead from the drop is via E&M DROP jack J4. The input voltage on the E lead is shifted 30 volts by Zener diodes CR4 or CR5 while that on the M lead is shifted 12 volts by CR6. In any E&M mode in the SEND-RCV position of S18, the termination is 1600 ohms provided by R5 and R3 in series. Regardless of the particular combination of open, battery, and ground supplied by the circuit under test, switches S18 and S19 connect the input and/or the internal battery and ground in such a manner that the top of R5 is always positive with respect to the bottom of R3 when current flows during the make (off-hook) interval.

4.48 On-hook/off-hook detection is accomplished by sensing current, or lack of current, through either R3, R3 plus R5, or the input resistance of the fast break detector. Current flows during the make (off-hook) interval but not during the break (on-hook) interval. When current flows, pin 1 of A6J3 is positive with respect to pin 2. When this is the case the output of limiter U7 goes high. Diodes CR8 through CR11 limit the input signal swing to 12 volts peak to peak. With the output of U7 high, the voltage at the non-interverting input of Schmitt trigger U6 exceeds the threshold voltage on the inverting input. The Schmitt trigger output rapidly switches to a high level and causes current to flow through the LED input half of opto isolator U14. The light from the LED turns on the photo transistor half and TP5 is pulled low. Thus for a make (off-hook) interval the voltage at TP5 is low. For a break (on-hook) interval there is no current through the terminating resistance and TP5 is pulled high through R12.

4.49 One of the requirements of the 1260A receiver is that it detect and measure percent break across contact suppression capacitance of up to two microfarads. During the break-to-make transition this capacitance is not a problem since it is rapidly charged through the pulsing contacts under test. Therefore, no significant distortion is introduced. During the make-to-break transition however, this capacitance must be discharged through the input resistance presented by the 1260A plus any contact suppression resistance. The effect is that the detected make-to-break transition occurs later than the original transition at the pulsing source and the break interval detected is distorted. It is the function of the fast break detector located on the analog receiver auxiliary assembly to minimize this distortion.

4.50 It will be recalled that during the make interval, the output of limiter U7 is high. This is applied to the reset input of one-shot U2, placing it in a mode where it can respond to an input trigger. Also, during the make interval the voltage on the non-inverting input of comparator U1 is more positive than the voltage on the inverting input and the comparator output is high. As the input voltage starts to decay during the make-to-break transition, capacitor C1 delays the decay at the inverting input of U1 with respect to the non-inverting input. The result is the voltage at the non-inverting input decays faster than that at the inverting input causing the comparator output to go low momentarily. This is used to trigger one-shot U2, which has a period of five milliseconds. The high Q output of U2 turns on Q1, which applies ground to the non-inverting input of Schmitt trigger U6 for five milliseconds. This immediately forces its output low, which is the break interval state. The five-millisecond period allows the input of limiter U7 to reach the normal break interval threshold of U6. During the break interval the output of the limiter is low and holds one-shot U2 reset.

4.51 The limiter, Schmitt trigger, and fast break detector are powered from a 12-volt floating power supply. This supply is comprised of U2B, U1, T1, diode rectifiers CR2 through CR5, and filter capacitor C1. The input to U2B is a 40-kHz squarewave. Complementary outputs of U2B are applied to the two inputs of driver U1. Transients at the outputs are limited to 12 volts peak-to-peak by diodes CR1 and CR7. Transformer T1 generates an isolated ac waveform at its secondary. This is rectified by the bridge rectifier and filtered by C1. The output voltage across +VI and −VI is approximately 12 volts dc.

4.52 The rise times of the opto isolator output are not fast enough for the TTL logic stages that follow it. Inverters U11C and U11D have Schmitt trigger input stages and produce outputs that have greatly reduced rise times. After two more inversions in U8B and U19E the waveform is applied to % BK meter M1. A make (off-hook) interval causes the meter to deflect full scale to indicate OFF HK. On the other hand, a break (on-hook) interval results in no current and the meter indicates ON HK.

4.53 The conversion technique used by the 1260A to generate digital words that are proportional to the received make and break intervals requires a frequency source of high precision. U18 is a combination oscillator and divide-by-64 stage that produces a 40-kHz squarewave output. Crystal Y1 operates at 2.56 MHz and determines the basic operating frequency before division. Inverters U17A through U17F and U19D decrease the rise times and furnish the required drive current. The 40-kHz waveform is used by the floating power supply, the debounce circuit, and the time interval-to-digital word converter.

4.54 A decision of major importance that must be made by the unit is that of determining conclusively when the input waveform has changed from make to break and vice-versa. In reality, the transitions are almost never clean but rather are usually accompanied by several cycles of contact bounce. This is particularly true of the break-to-make transition. It is the function of the debounce circuit to remove the effects of this contact bounce and generate a replica of the make and break intervals that have clean, well-defined edges.

4.55 See Figure 4−5 for a typical timing diagram for the debounce circuit. One break and one make interval, each with contact bounce, is shown. This requires the detection and regeneration of three edges. As a starting point it is assumed that flip-flops U3A and U2A are cleared and that the clock input to U3A is in a steady make state. The first break-to-make transition of the input sets U3A and causes its Q output to go high. It should be noted that the first transition is always assumed to be the only one, whether it is followed by bounce or not, before starting the debounce timeout interval.

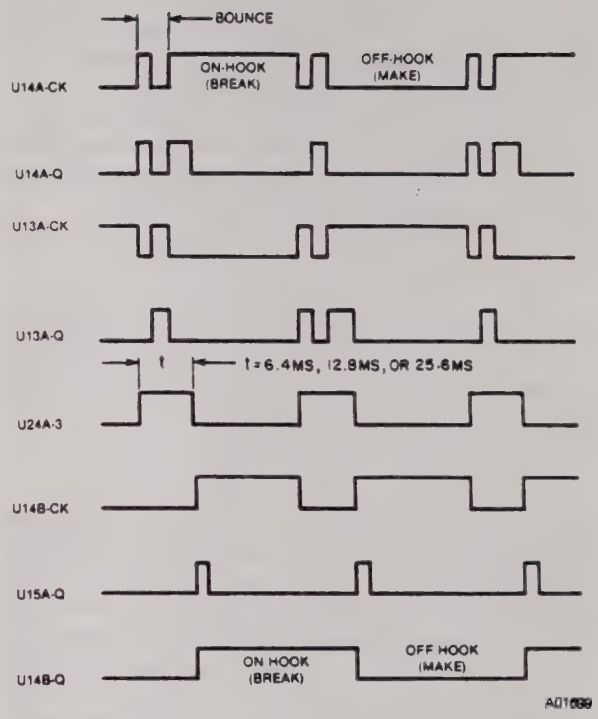


Figure 4−5. Debounce Circuit Timing Diagram.

4.56 The clock input of U3A is inverted by U8B and becomes the clock input for the U2A. This arrangement assures that every edge, including contact bounce, of the input signal is detected. The first contact bounce transition is used to clock U2A and its Q output goes high. This is inverted by U8C and clears U3A, forcing its Q output low. The high Q output of U2A is applied through U8A and U10A to keep U10B enabled, thus continuing the debounce period.

4.57 The next bounce transition sets the Q output of U3A high. This clears U2A through U8D and also keeps U10B enabled. After counting 256 pulses the 2QD output of U9 goes low. The time required to count 256 pulses depends on the position of internal debounce interval switch S1. This allows a debounce period of either 6.4, 12.8, or 25.6 milliseconds to be selected. Flip-flop U12B is a divide-by-two stage. The output of U9 is inverted by U10C to clock U3B and trigger 50-microsecond one-shot U15. If the input signal at the ouput of U11D is still high, i.e. completion of bounce, U3B will be set and its Q output will go high. The 50-microsecond pulse generated by U15 is used to clear U3A.

4.58 The debounce circuit is again in a steady state awaiting the first make-to-break transition. This transition will be detected by U2A and start the debounce period as just described. At the end of the debounce period, and if no more bounce is present, U3B will be cleared and its Q ouput will go low.

4.59 The effect of the debounce circuit is to generate, at the Q output of U3B, a replica of the input free of any contact bounce. If bounce is present longer than the selected debounce period the bounce will be carried through to the output of U3B. The output of U3B is buffered by U11A before being applied to the digital section of the receiver.

4.60 DIGITAL SECTION OF THE RECEIVER

4.61 The digital section of the receiver is comprised of an address decoder, edge detectors, and a time interval-to-digital converter. These circuits are shown on the right-hand page of Figure 6—2.

4.62 **Address Decoder**

4.63 The address decoding utilizes certain memory address locations placed on the address bus by the software to control the events occurring during the time of interval-to-digital conversion. Address bits A0 through A4 and A8 through A15, in conjunction with control lines HLDA and MEMR, are used for address decoding. These are all outputs of CPU U9 and system controller U7 located on A8. The HLDA output of U9 is always in the non-active or low state. This is used to permanently enable tri-state bus drivers U4, U5, and U6.

4.64 Address bits A8 through A15 are buffered by U5 and U6 and then applied to open collector AND gates U2A, U2B, and U2C. When A8 through A15 are all high, the AND gate output goes high, is buffered in U4, and appears as an output line designated I/O. This corresponds to memory locations FFXXH and has been chosen to enable the I/O ports used in the 1260A. The remaining five bits are buffered in U4 and U5 and are then designated AB0 through AB4. They form the XX parts of the general FFXXH locations. The final line used in decoding is MEMR that is present at the output of U7 anytime there is a read command.

4.65 Address decoder U33 located on A7 is a device that has two enable inputs and three binary inputs. When the G1 enable is high and the G2A/B enable is low, the Y outputs go low one at a time in accordance with the binary input code. Table 4—3 shows how these inputs are decoded to form FF08H(R), FF09H(R), FF0AH(R), FF0BH(R), FF0CH(R), and FF0DH(R).

Table 4—3. Receiver Address Decoding Truth Table.

$\overline{\text{MEMR}}$	I/O	AB4	AB3	AB2	AB1	AB0	FF08H(R)	FF09H(R)	FF0AH(R)	FF0BH(R)	FF0CH(R)	FF0DH(R)
L	H	L	H	L	L	L	L	H	H	H	H	H
L	H	L	H	L	L	H	H	L	H	H	H	H
L	H	L	H	L	H	L	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H
L	H	L	H	H	L	L	H	H	H	H	L	H
L	H	L	H	H	L	H	H	H	H	H	H	L

4.66 Edge Detectors and Time Interval-To-Digital Converter

4.67 The edge detectors and time interval-to-digital converter generate 16-bit binary words that represent the break and make time intervals. These words are then used by the processor to compute the pulsing speed and percent break and to ultimately display the results.

4.68 The 40-kHz pulses from A6 are inverted by U37B and applied to U36A. The debounced analog receive signal in inverted by U37A and applied to U36B. At the time a reset pulse is generated at power on, FF0AH(R) goes low to preset U32B. This sets the Q output high to enable both U36A and U36B for all normal operating modes. Thus 40-kHz pulses and the analog signal are applied to the counters and edge detector all of the time.

4.69 See Figure 4—6 for the event sequence diagram that represents the time interval-to-digital conversion function. This conversion process can be represented by considering what happens to an on-hook (break) interval followed by an off-hook (make) interval. On the diagram these are represented by t_1 and t_2, which are defined by edges E1, E2, and E3.

4.70 Edge detectors U34B and U34A are five-microsecond one-shots. Each negative edge of the analog signal triggers U34A, which produces a negative pulse at its Q output. Each positive edge, on the other hand, triggers U34B. When the outputs of these two one-shots are applied to OR gate U36D, the OR gate has one positive pulse for each edge of the analog signal.

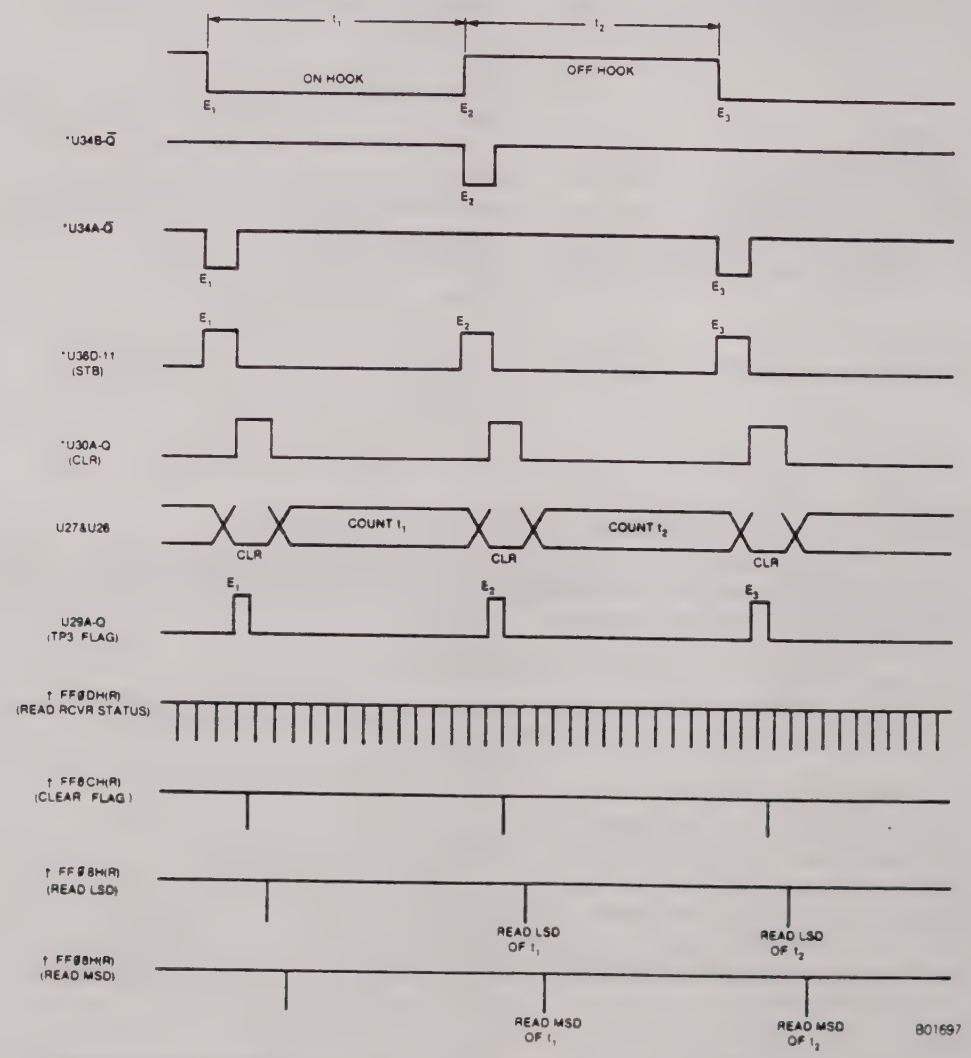


Figure 4—6. Event Sequence Diagram for the Receiver Time Interval-To-Digital Converter.

4.71 These positive pulses are used to trigger one-shot U30A and strobe the counter data into the I/O ports. The 5-microsecond positive pulse present at the Q output of U30A is used to clear the counters to zero and to set flag flip-flop U29A. The result so far in the process of converting t_1 to a digital word is as follows:

1. Edge E1 has been detected;

2. Then, five microseconds later, the counters are cleared to zero so that they immediately begin to totalize 40-kHz pulses for the measurement of t_1;

3. The receive flag, as present at TP3, is set high to alert the processor to the fact that an edge has occurred.

4.72 Approximately once each millisecond, the interrupt service routine causes FF0DH(R) to go low. This enables tri-state bus drivers in U25 and the receive flag, and the state of the analog signal at that instant is placed onto the data bus for application to the processor. The presence of the flag causes the software to assume temporary control of the digital receiver operation. The level of the analog signal just after the edge was detected is called the tip-ring status and is used by the processor to determine if the previous interval just measured was break or make. Very soon, FF0CH(R) goes low to clear the flag flip-flop in anticipation of detecting edge E2.

4.73 The detection of E2 signals the end of t_1 and the following events occur. The positive pulse at the output of U36D strobes the t_1 count accumulated by U27 and U26 into I/O ports U24 and U23. The data does not appear on the bus as yet. Five microseconds later the counters are cleared to zero and start to totalize the count for t_2. Also, the flag is again set at this time. After FF0DH(R) and FF0CH(R) read and clear the flag respectively, the data representing t_1 is now ready to be placed on the data bus. In rapid succession FF08H(R) and FF09F(R) go low and read the eight least significant bits and the eight most significant bits onto the bus.

4.74 The t_2 data count is next terminated with the detection of edge E3. Operation is as previously described, and the digital word is placed on the bus. All data on the bus is buffered by system controller U7 located on A8. The buffered data is then applied to the CPU for use in computations.

4.75 INTERRUPT AND DISPLAY BLOCK DIAGRAM DESCRIPTION

4.76 See Figure 4—7 for a simplified block diagram of the interrupt and display functional section. The purpose of the section is to continuously generate a repetitive interrupt signal and to display the pulsing speed and percent break data.

4.77 Addresses supplied by the processor are decoded and used to trigger an interrupt one-shot and to latch display data. Four of the latched bits are decoded and used to drive the seven-segment display. Three more bits are decoded and used to multiplex the data among the six digits of the display.

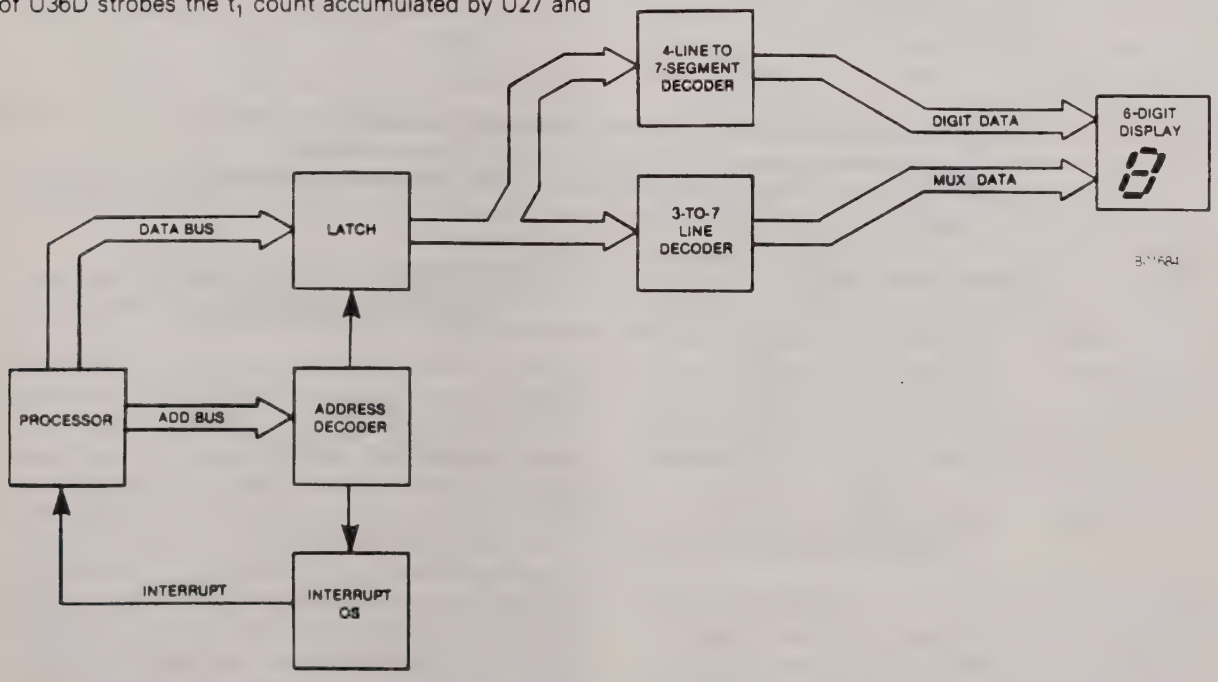


Figure 4—7. Interrupt and Display Block Diagram.

4.78 INTERRUPT AND DISPLAY DETAILED CIRCUIT DESCRIPTION

4.79 See Figure 6–3 for the functional schematic diagram of the interrupt and display function. Separate descriptions of the address decoding, interrupt generation, and display updating subfunctions are presented in the following paragraphs.

4.80 ADDRESS DECODER

4.81 The address decoding utilizes certain memory address locations placed on the address bus by the software to control the events occurring during the interrupt and display function.

4.82 Address bits A0 through A4 and A8 through A15, in conjunction with control lines HLDA and $\overline{\text{MEMW}}$, are used for address decoding. These are all outputs of CPU U9 and system controller U7 located on A8. The HLDA output of U9 is always in the nonactive or low state. This is used to permanently enable tri-state bus drivers U4, U5, and U6.

4.83 Address bits A8 through A15 are buffered by U5 and U6 and then applied to open collector AND gates U2A, U2B, and U2C. When A8 through A15 are all high, the AND gate output goes high, is buffered by U4, and appears as an output line designated I/O. This corresponds to memory locations FFXXH and has been chosen to enable the I/O ports used in the 1260A. The remaining five bits are buffered in U4 and U5 and are then designated AB0 through AB4. They form the XX bits of the general FFXXH locations. The final line used in decoding is $\overline{\text{MEMW}}$ that is present at the output of U7 anytime there is a write command.

4.84 Address decoder U16 is a device that has two enable inputs and three binary inputs. When the G1 enable is high and the G2A/B input is low, the Y outputs go low one at a time in accordance with the binary input code. Table 4–4 shows how these inputs are decoded to form FF03H(W) and FF04H(W).

Table 4–4. Interrupt and Display Address Decoding Truth Table.

$\overline{\text{MEMW}}$	I/O	AB4	AB3	AB2	AB1	AB0	FF03H(W)	FF04H(W)
L	H	L	L	L	H	H	L	H
L	H	L	L	H	L	L	H	L

4.85 INTERRUPT GENERATION

4.86 In the 1260A the interrupt cycle is self-perpetuating and is designed to occur once every millisecond. Whenever an interrupt command is generated, the processor enters an interrupt mode and the main program vectors to an interrupt service routine. During the execution of this service routine, the transmitter, receiver, and the dial keypad are serviced, if they request it, and the display is updated.

4.87 The interrupt cycle gets its start at power-on, at which time a reset command is generated. The most convenient starting point at which to begin discussion of the interrupt cycle is to assume that it is presently in the interrupt mode. This is represented by a low INTR line at the Q output of U13A. See Figure 4–8 for the interrupt cycle event sequence diagram.

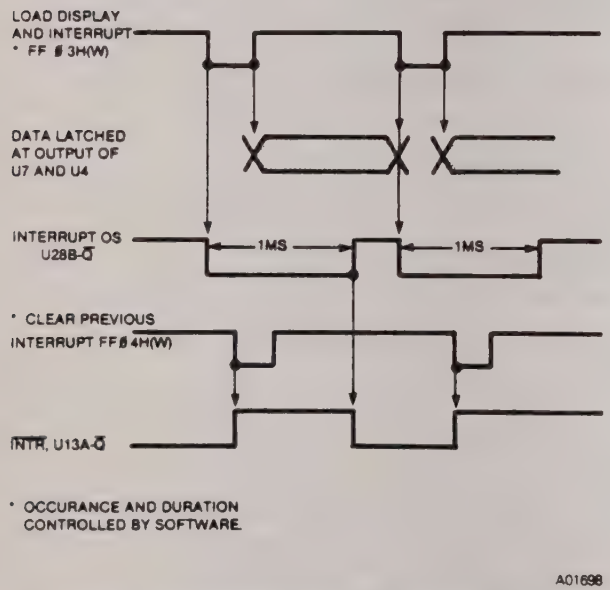


Figure 4–8. Event Sequence Diagram for the Interrupt and Display Function.

4.88 While the CPU is executing the interrupt service routine, a write command to memory location FF03H is given. This is decoded and appears at FF03H(W) at the trigger input to one-shot U28B. The negative leading edge triggers the one-shot, which requires one millisecond to time out. During this time, the subroutine issues a write command to memory location FF04H. This is decoded and, as FF04H(W), clears the previous interrupt by clearing U13A. At the end of one millisecond, the positive edge of the one-shot output clocks U13A and the INTR line goes low to again place the CPU in the interrupt mode. The appearance of the next FF03H(W) signal triggers the one-shot and the cycle repeats.

4.89 DISPLAY UPDATING

4.90 The eight data bits at the D outputs of U9 on A8 are buffered in system controller U7 and then placed on the data bus. Bits DB0 through DB3 carry the character information in binary format. The multiplex information in binary format is represented by DB4, DB5, and DB6.

4.91 Tri-state bus drivers U10 and U1 located on A7 are permanently enabled since their G1/2 inputs are strapped to ground. Thus, whatever is present on the data bus is always present at the inputs to latches U7 and U4. Approximately once each millisecond, FF03H(W) goes low for a short period of time. The leading edge of this signal allows data to enter U7 and U4 but is not latched and thus is not yet present at the outputs. When FF03H(W) returns to the high state, the data is latched and applied to U8 and U7 located on A11A2.

4.92 The four-line to seven-segment decoder U8 converts the four-line BCD input data to a seven-segment code that determines the character to be displayed. See Table 4–5. The decoder outputs are applied through current limiting resistors to the six LED displays in parallel.

4.93 The particular LED display lighted at any instant is the function of three-line to seven-line multiplex decoder U7. The three-line binary input causes the outputs to go low one at a time as shown in Table 4–6. The selected low output saturates its associated transistor and + 5 V dc is applied to the corresponding LED display. Each LED display is turned on for one millisecond and turned off for six milliseconds. This reduces the current drain on the + 5 V dc power supply. Decimal points for U1 and U4 are normally lighted by being connected to ground through COUNT-ID-DIGITS switch S2 located on the front panel. When this switch is depressed and held, these decimal points are turned off as they are not appropriate for these display functions. The decimal point associated with U6 is used as an over range indicator for digit positions 10 through 16 when in this display mode. This decimal point is lighted when the Y6 output of U7 is low. This turns on Q5, which in addition to enabling U6, applies + 5 V dc through R7 and CR1 to turn on Q7. The ground applied by this stage lights the decimal point. Since Q5 is also turned on by the Y0 output of U7, the decimal point is inhibited by the low Y0 line through CR2.

4.94 **DIAL KEYPAD DATA ENTRY BLOCK DIAGRAM DESCRIPTION**

4.95 See Figure 4–9 for a simplified block diagram of the dial keypad functional section. The purpose of this functional section is to convert 1-out-of-12 data supplied by the dial keypad into BCD data that is then placed on the data bus for use by the processor

4.96 When any of the dial keypad pushbuttons is pressed, the 1-out-of-12 data is converted to BCD data in an encoder. The encoder output is used to generate a keypad flag and to latch itself into the I/O port. Software now takes control to read the flag, place the data on the bus, and clear the flag at the completion of the cycle. Software control is exercised through the process of decoding certain memory addresses.

Table 4—5. Four-Line to Seven-Segment Decoding Truth Table.

DISPLAY	U8										
	D	C	B	A	a	b	c	d	e	f	g
0	L	L	L	L	L	L	L	L	L	L	H
1	L	L	L	H	H	L	L	H	H	H	H
2	L	L	H	L	L	L	H	L	L	H	L
3	L	L	H	H	L	L	L	L	H	H	L
4	L	H	L	L	H	L	L	H	H	L	L
5	L	H	L	H	L	H	L	L	H	L	L
6	L	H	H	L	H	H	L	L	L	L	L
7	L	H	H	H	L	L	L	H	H	H	H
8	H	L	L	L	L	L	L	L	L	L	L
9	H	L	L	H	L	L	L	H	H	L	L
C	H	L	H	L	H	H	H	L	L	H	L
-	H	H	L	H	L	H	H	L	H	L	L

Table 4—6. Three-Line to Seven-Line Multiplex Decoding Truth Table.

DIGIT ON	U7									
	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6
U6	L	L	L	L	H	H	H	H	H	H
U5	L	L	H	H	L	H	H	H	H	H
U4	L	H	L	H	H	L	H	H	H	H
U3	L	H	H	H	H	H	L	H	H	H
U2	H	L	L	H	H	H	H	L	H	H
U1	H	L	H	H	H	H	H	H	L	H
U6 and DP	H	H	L	H	H	H	H	H	H	L

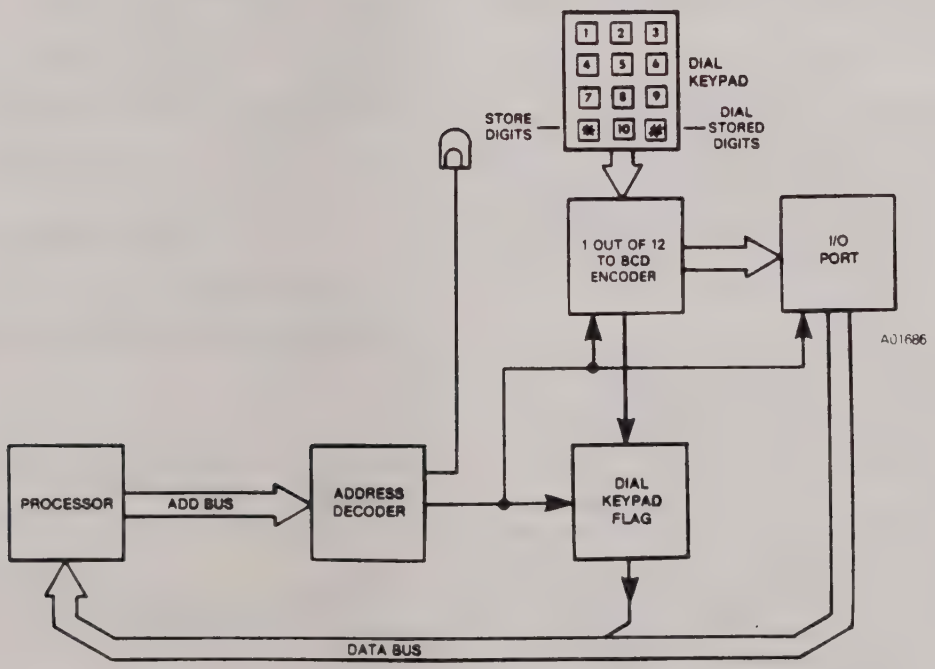


Figure 4—9. Dial Keypad Data Entry Block Diagram.

4.97 DIAL KEYPAD DATA ENTRY DETAILED CIRCUIT DESCRIPTION

4.98 See Figure 6—4 for the functional schematic diagram of the dial keypad data entry function. Figure 4—10 illustrates the sequence of events that occur during the processing of dial keypad data onto the bus. Table 4—7 is a truth table for address decoding and Table 4—8 is a truth table for the 1-out-of-12-to-BCD encoding scheme.

4.99 Dial keypad S17 is a 1-out-of-12 device with the selected line at ground. The selected line is then immediately converted to four-line BCD by priority encoders U19 and U20 located on A7. All inputs are connected to + 5 V dc through pull-up resistors. Priority encoder outputs are active low as shown on the truth table.

4.100 BCD data is applied to inputs of U22 through U21A, B, and D. Any time a pushbutton is pressed, the output of U21C immediately goes high and triggers 50-millisecond one-shot U30B. The trailing edge of the Q output strobes and latches the BCD data into U22 but the data is not yet placed on the bus. The trailing edge of the Q output clocks U32A and, if the output of U21C is still high, the flag flip-flop is set and its Q output goes high.

4.101 Approximately once each millisecond, FF0DH (R) goes low and U25A places the flag on the data bus via D87. When the processor is ready to receive the keypad data, FF0EH(R) goes low. This is inverted by U35B to enable the outputs of I/O port U22. The BCD data is now on the data bus. After the processor has finished with the keypad data, FF0FH(R) goes low to clear flag flip-flop U32A and the cycle is now complete.

4.102 The storage and the automatic outpulsing of digits is controlled by the * and # keys respectively. Once initiated by the appropriate key, the associated functions are entirely under software control. The first time that the * key is pressed the store digits mode is initiated. The FF05H(W) output of U16 on A7 then goes low. This is inverted by U11B on A6, and clocks U12A. The D input of this flip-flop is DB0 and will be high the first time it occurs. The Q output of U12A goes low and the STORE DIGITS indicator on the front panel is lighted. The software causes FF05H(W) to be generated approximately once a second for 10 seconds while DB0 alternates from high to low. This causes the STORE DIGITS indicator to flash. During this 10-second flashing period the digits to be stored can be entered. A maximum of 16 digits can be entered and stored. If less than 16 digits are entered, the indicator will be lighted continuously after the 10-second timeout interval or if the * key is pressed a second time. It is also lighted continuously immediately after entering the sixteenth digit. After the desired digits have been entered and stored they will be automatically outpulsed when the # key is pressed. This can be repeated as many times as desired. The stored digits can be cleared from memory by again pressing the * key. The STORE DIGITS indicator will again flash indicating that new digits can be entered and stored. If none are desired, the store function can be cancelled by again pressing the * key or waiting for the 10-second timeout. When the unit is powered up, RESET goes low and clears U12A on A6. This ensures that the unit starts up in the non store digits mode.

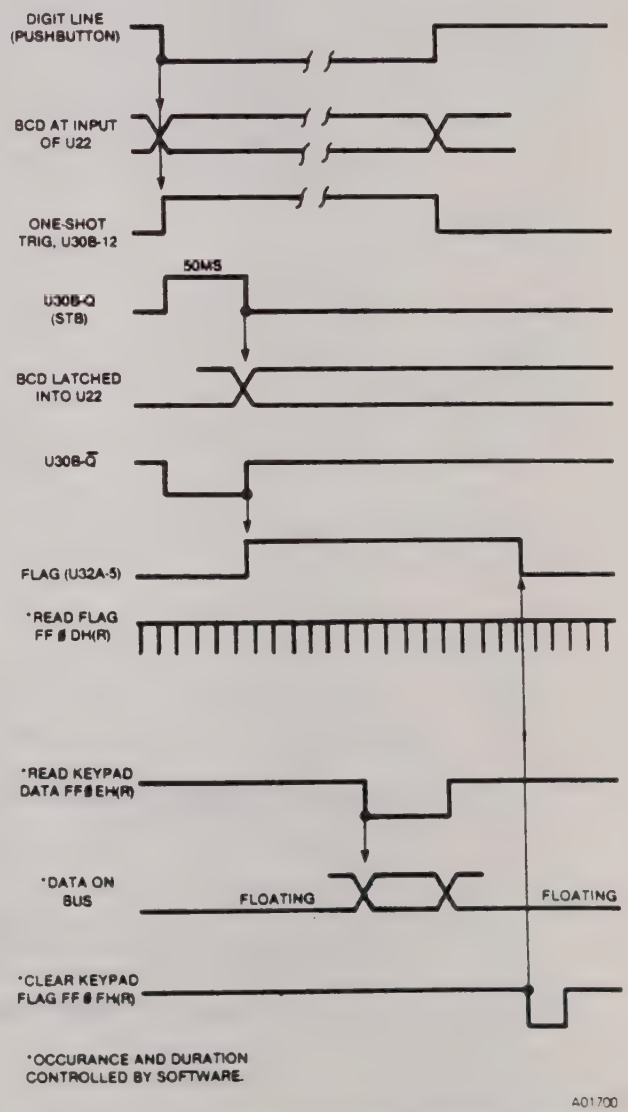


Figure 4—10. Event Sequence Diagram for the Dial Keypad Entry Function.

Table 4—7. Dial Keypad Data Entry Address Decoding Truth Table.

MEMR	I/O	AB4	AB3	AB2	AB1	AB0	FF0DH(R)	FF0EH(R)	FF0FH(R)
L	H	L	H	H	L	H	L	H	H
L	H	L	H	H	H	L	H	L	H
L	H	L	H	H	H	H	H	H	L
MEMW	**I/O**	**AB4**	**AB3**	**AB2**	**AB1**	**AB0**	**FF05H(W)**		
L	H	L	L	H	L	H	L		

Table 4—8. 1-Out-of-12 to BCD Encoding Truth Table.

DIGIT	U19			U20				U22			
	A0	A1	A2	A0	A1	A2	E0	DI1(1)	DI3(2)	DI4(4)	DI2(8)
1	L	H	H	H	H	H	L	H	L	L	L
2	H	L	H	H	H	H	L	L	H	L	L
3	L	L	H	H	H	H	L	H	H	L	L
4	H	H	L	H	H	H	L	L	L	H	L
5	L	H	L	H	H	H	L	H	L	H	L
6	H	L	L	H	H	H	L	L	H	H	L
7	L	L	L	H	H	H	L	H	H	H	L
8	H	H	H	H	H	H	H	L	L	L	H
9	H	H	H	L	H	H	H	H	L	L	H
0	H	H	H	H	L	H	H	L	H	L	H
*	H	H	H	L	L	H	H	H	H	L	H
#	H	H	H	H	H	L	H	L	L	H	H

4.103 SWITCH STATUS BLOCK DIAGRAM DESCRIPTION

4.104 See Figure 4—11 for a simplified block diagram of the switch status function. The purpose of this function is to keep the processor informed of the status of the MAX, MIN, COUNT-ID-DIGITS, ON HOOK/OFF HK-DIAL/CONT, SPEED, % BREAK and ID switches. When the processor is ready to poll a particular switch, a corresponding address is placed on the address bus. This is decoded in an address decoder, which enables the bus driver associated with the switch of interest. The data bus carries the information to the processor where it is used.

4.105 SWITCH STATUS DETAILED CIRCUIT DESCRIPTION

4.106 See Figure 6—5 for the functional schematic diagram of the switch status function. This function consists of the address decoder and a bus driving system described in the following paragraphs.

4.107 ADDRESS DECODER

4.108 The address decoder utilizes certain memory address locations placed on the address bus by the software to control the events occurring during the process of monitoring the switch status. Address bits A0 through A4 and A8 through A15, in conjunction with control line $\overline{\text{MEMR}}$, are used for address decoding. These are outputs of CPU U9 and system controller U7 located on A8. The HLDA output of U9 is always in the non-active or low state. This is used to permanently enable tri-state bus drivers U4, U5, and U6.

4.109 Address bits A8 through A15 are buffered by U5 and U6 and then applied to open collector AND gates U2A, U2B, and U2C. When A8 through A15 are all high, the AND gate output goes high, is buffered by U4, and appears as an output line designated I/O. This corresponds to memory locations FFXXH and has been chosen to enable the I/O ports. The remaining five bits are buffered in U4 and U5 and are then designated AB0 through AB4. They form the XX parts of the general FFXXH locations. The final line used in decoding is $\overline{\text{MEMR}}$ that is present when there is a read command.

4.110 Address decoder U2 located on A6 is a device that has two enable inputs and three binary inputs. When the G1 enable is high and the G2A/B enable is low, the Y outputs go low one at a time in accordance with the binary inputs. Table 4—9 shows how these inputs are decoded to form the five I/O commands.

4.111 LINE DRIVERS

4.112 See Figure 6—5 for the functional schematic diagram of the switch status function. The SPEED, % BREAK and ID thumbwheel switches located on the front panel provide BCD outputs. The active lines are grounded and the others are open. The MIN, MAX, and the ON HOOK/OFF HK-DIAL/CONT switches apply ground to the selected line while the COUNT-ID-DIGITS switch removes ground. All of these lines are hard wired to tri-state bus drivers located on A6. All of the bus driver inputs, including unused inputs, are tied to the + 5 V dc supply through pull-up resistors.

4.113 When a low level I/O command is applied to the bus drivers, the BCD information is placed on an internal data bus and then on the general data bus through isolation resistors. Selection of which switch gets read onto the data bus in under software control.

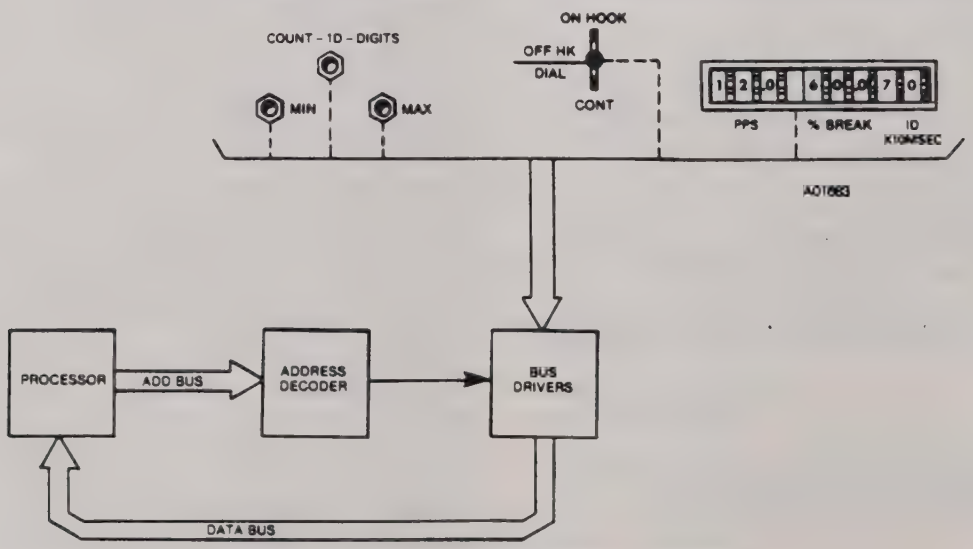


Figure 4—11. Switch Status Block Diagram

Table 4—9. Switch Status Address Decoding Truth Table.

I/O	$\overline{\text{MEMR}}$	AB0	AB1	AB2	AB3	AB4	FFXXH(R)	READ SWITCH STATUS FOR
H	L	H	H	L	L	H	FF13H(R)	ON HOOK/OFF HK-DIAL/CONT, MIN and MAX
H	L	L	L	H	L	H	FF14H(R)	% BREAK X 10^1 and X 10^0
H	L	H	L	H	L	H	FF15H(R)	% BREAK X 10^{-1} and PPS X 10^{-1}
H	L	L	H	H	L	H	FF16H(R)	PPS X 10^1 and X 10^0
H	L	H	H	H	L	H	FF17H(R)	ID X 10^2 and X 10^1

4.114 MONITOR BLOCK DIAGRAM DESCRIPTION

4.115 See Figure 4—12 for a simplified block diagram of the monitor function. The purpose of the monitor function is to visually display the supervision status of the circuits under test connected to the three front panel jacks. The sleeve of the LOOP RCV jack is monitored and the associated indicator is lighted when the sleeve is grounded. When the E&M jacks are monitored they are connected in parallel so that they are in the through mode. When the E lead is not grounded the E indicator is lighted. When the M lead is not at battery potential the M indicator is lighted.

4.116 MONITOR DETAILED CIRCUIT DESCRIPTION

4.117 See Figure 6—6 for the functional schematic diagram of the monitor function. The monitor circuit for both the LOOP RCV and the E&M LINE jacks are identical with one minor exception. The sleeve detector has an additional inverter stage so that the associated indicator is lighted in the presence of ground while the E lead detector causes its associated indicator to light in the absence of ground. The sleeve detector will be described as representative of the two.

4.118 When the sleeve of LOOP RCV jack J2 is either open or at battery potential Q4 is held cut off by − 48 V dc through R27. With no current through the LED half of opto isolator U16 the photo transistor half is cut off and the input of U11C is pulled high through R60. After two inversions in U11C and U5A the cathode of SLEEVE GND indicator DS3 is a high and the indicator is not lighted. On the other hand when the sleeve is grounded, Q4 conducts and the opto isolator pulls the input of U11C low. Inverter U5A provides the drive current to light DS3. A lighted SLEEVE GND indicator indicates a busy loop while a lighted E indicator indicates an idle E lead.

4.119 When the M lead of E&M DROP jack J4 is at battery potential transistors Q6 and Q5 are turned on and current flows through the LED half of opto isolator U15. The photo transistor half pulls the input of U5C to ground. The high inverter output keeps M indicator DS2 from being lighted. On the other hand when the M lead is either open or grounded, there is no current to operate the opto isolator and the input of U5C is pulled high through R3. The inverter output grounds the cathode of M indicator DS2 and the indicator is lighted. This indicates an idle M lead.

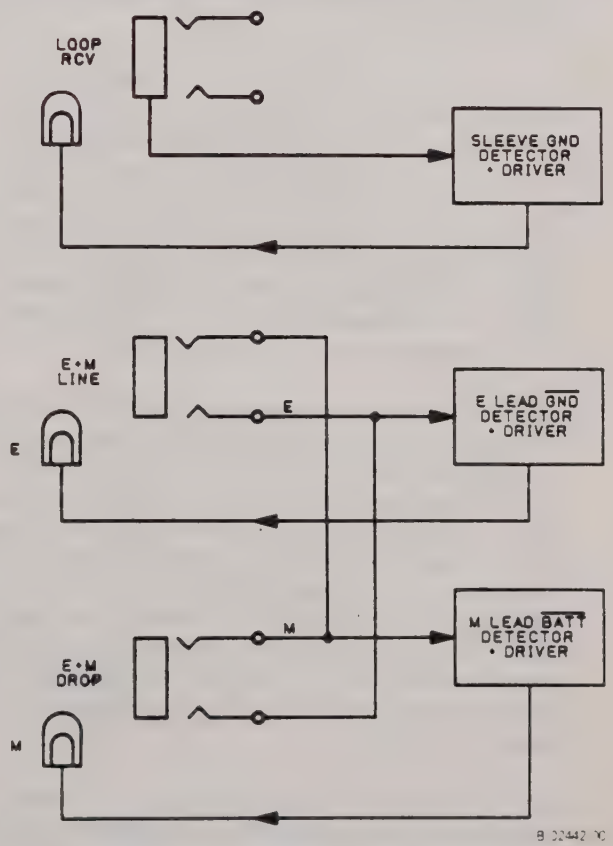


Figure 4—12. Monitor Block Diagram.

4.120 RESET BLOCK DIAGRAM DESCRIPTION

4.121 See Figure 4—13 for a simplified block diagram of the reset function. The purpose of the reset initialize is to initiate the software so that it is in synchronization with the hardware, particularly when power is first applied to the unit. There are two ways in which to generate a reset pulse at the input of the CPU. The first and most common is via the power on detector whenever the POWER switch is set to the ON position. The second is by pressing the internally mounted reset switch. This switch is provided only as a trouble-shooting convenience. In both cases the CPU and an associated bootstrap flip-flop initialize the stored program.

4.122 RESET DETAILED CIRCUIT DESCRIPTION

4.123 See Figure 6—7 for the functional schematic diagram of the reset function. There are two conditions for the reset pulse at $\overline{\text{RESIN}}$ input pin 2 of clock generator U8 located on A8. The first condition is that generated by RC network R4-C8. When power is first applied the + 5 V dc comes up immediately, but C8 charges slowly through R4. This allows the Schmitt trigger input of U8 to internally generate a reset pulse. The second way of producing a reset pulse is to momentarily press S1 on A8. As a result of either of these reset pulses, U8 provides a positive edge at RESET output pin 1.

4.124 Any reset pulse immediately causes CPU U9 to attempt to read the first instruction stored in memory. To do this the CPU places address code 0000H on the address bus. This is the first memory location in RAM, but it is desired to read the first instruction stored in PROM U9. This is done by momentarily forcing the address decoder located on the memory board to decode memory location 8000H, which is the first location in PROM U9. This memory location contains an instruction that gets the program started correctly.

4.125 The same positive edge at the RESET output of clock generator U8 is inverted by U3C and applied to the bootstrap flip-flop located on A9. The bootstrap is set and its output goes positive. This then becomes a substitute for AB15, the most significant bit of the address, and is applied through U5D to the SEL B input of U6. Along with AB10 through AB15, all of which are low, the SEL B input causes the 2Y2 output to go low and select PROM U9. Since AB0 through AB9 are all low, the cumulative effect is that the instruction stored in memory location 8000H is placed on the data bus and applied to the CPU.

4.126 Now that the CPU has been given a reliable instruction to start the program, it is necessary to free up the operation of AB15 at the input to U5D on A9. After executing further instructions, the CPU causes system controller U7 to issue a $\overline{\text{MEMW}}$ write command. This low level resets the bootstrap flip-flop, whose output goes low and frees AB15 so that this bit has control when required. The bootstrap remains in this state until another reset pulse is generated.

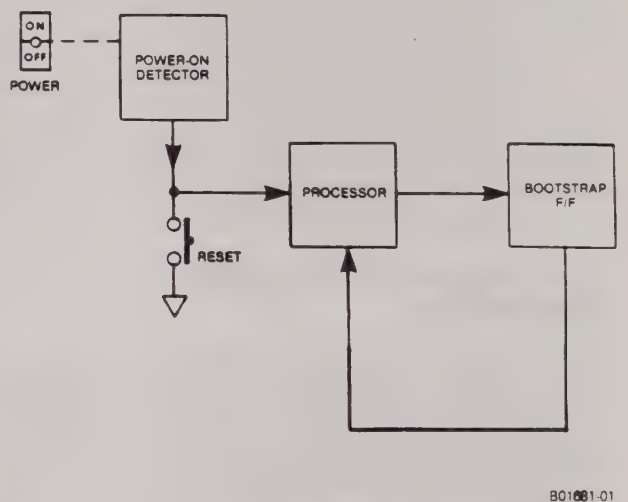


Figure 4—13. Reset Block Diagram.

4.127 SF ADAPTER OPTION 1260-10 CIRCUIT DESCRIPTION

4.128 The SF adapter provides the basic 1260A Pulsing Test Set with the capability of sending and receiving SF signaling. It is a plug-in module that can be inserted into either of the two front panel slots.

4.129 SF SEND BLOCK DIAGRAM DESCRIPTION

4.130 See Figure 4—14 for the simplified block diagram of the SF send function. The send circuit is functionally a dial pulse-to-SF converter. The 2600/2400-Hz oscillator generates the basic SF tone. As an alternative an external SF tone can be connected via the EXT OSC jack. The SF tone is gated with the output of the 1260A transmitter, which also determines the pulse speed, percent break, interdigit time, and dialed digits. The final stage is a variable-gain amplifier. When sending toward the drop the signal level is above the line level 23 dB. In addition, the SF pulsing-level is 12 dB above the idle on-hook level. The output is available at the SF SEND jack.

4.131 SF SEND DETAILED CIRCUIT DESCRIPTION

4.132 See Figure 6—8 for the functional schematic diagram of the SF send section. The SF send section is comprised of an SF tone source, gating circuits, and amplifier/gain adjusting circuits.

4.133 SF Tone Source

4.134 The SF tone source is a Wien bridge oscillator using amplitude stabilization. The frequency-determining components within the bridge are resistors R1, R5, R6, and R13 through R15, and capacitors C3 and C4. Switch sections S1-1 and S1-2 allow the output to be set to either of the two standard SF tones of 2400 or 2600 Hz. These frequency-determining components are located in the positive feedback loop of amplifier U1. Amplitude stabilization is a function of resistors R3, R32, and the drain-to-source resistance of Q2, all of which are located in the negative feedback path of U1. The drain-to-source resistance of Q2 is controlled by the dc voltage derived from a sample of the oscillator output signal level. The output of U1 is amplified by U3 and then converted to a proportional negative dc voltage by voltage doubler rectifier CR2, CR3, C7, and C6. The drain-to-source resistance is then varied so that it opposes any change in the output level of the oscillator. The SF output is then applied to a 16-position voltage attenuator. This provides levels at the SF SEND jack ranging from 7 dB above to 11 dB below the normal 4W circuit TLP levels obtained when S3 is set to the 0 dB position. Table 4—10 lists the supervision and pulsing levels provided by the SF module.

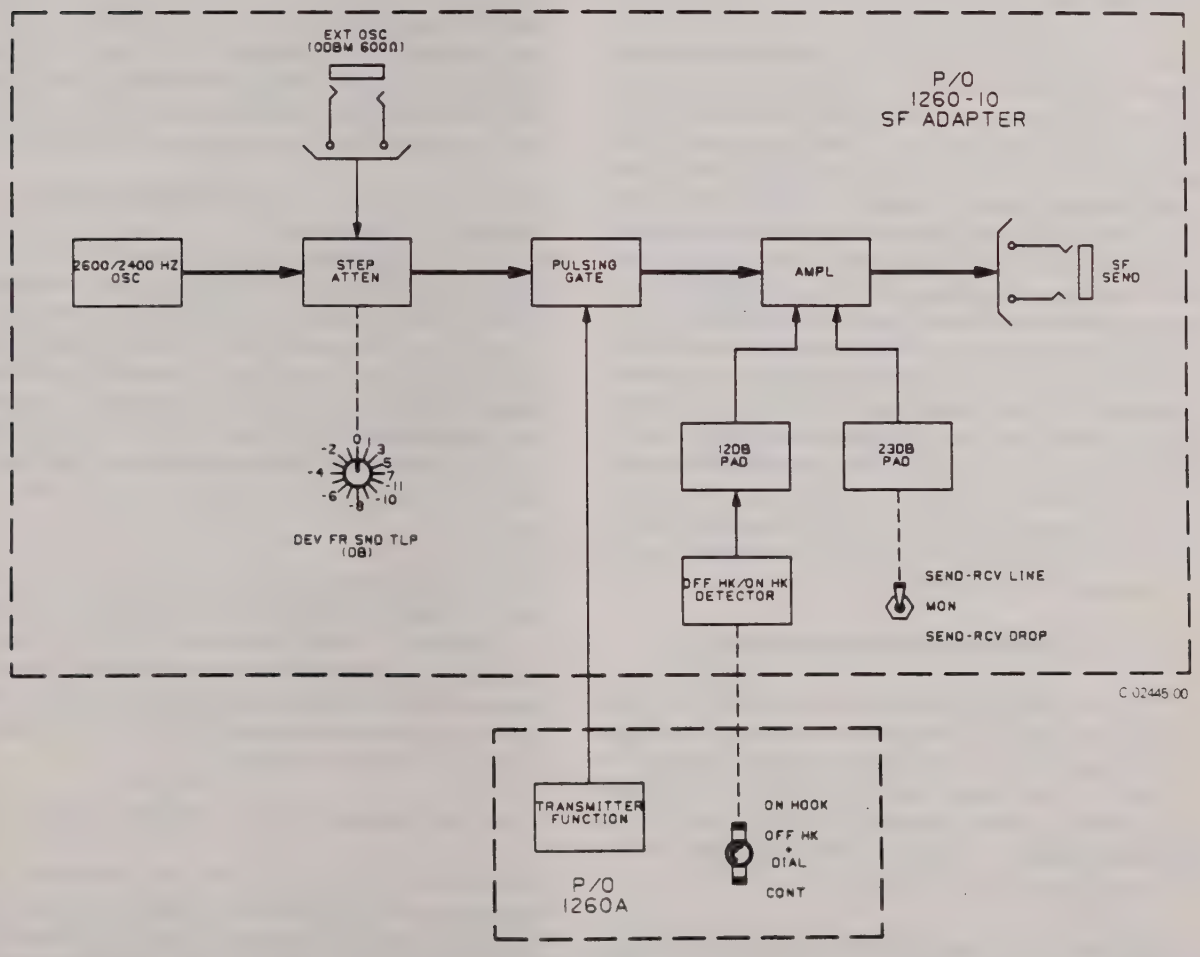


Figure 4—14. SF Send Block Diagram.

Table 4—10. SF Levels at 0 dB Position of S3.

	ON HOOK	ON HOOK WITH SF AUG	PULSING
TOWARD LINE	– 36 dBm	– 24 dBm for 400 ms after on hook; then – 36 dBm.	– 24 dBm
TOWARD DROP	– 13 dBm	– 1 dBm for 400 ms after on hook; then – 13 dBm.	– 1 dBm

4.135 **Gating Circuits**

4.136 The SF pulsing source is derived from the transmit signal of the 1260A. When SEND switch S20 on the 1260A is set to the E(SF)G&B position and when there is a plug inserted in the SF SEND jack, ground and battery pulsing is provided by the 1260A. The pulse speed, percent break, interdigit time, and dialed digits are determined by the 1260A controls. During the time the input is grounded, which corresponds to an off-hook interval, pulsing detector Q1 is cut off. SF gate Q3 is now pinched off by the negative voltage applied to the gate through R33 and CR14 cutting off any SF output. During the time the 1260A output is at battery potential, Q1 conducts and applies a positive voltage to CR14. The diode is reverse biased allowing normally conducting Q3 to provide an SF output. When SEND-RCV LINE/MON/SEND-RCV DROP switch S2 is set to the MON position, a negative voltage is applied through K1 and CR3 to pinch off Q3. This prevents cross talk to the receiver when monitoring a line.

4.137 **Amplifier/Gain Adjusting Circuits**

4.138 SF signaling specifications require that on-hook and pulsing levels be different when sending toward the line as opposed to when sending toward the drop. In addition, on-hook levels are maintained at pulsing levels for a period of time following an on-hook when using SF augmentation. These functions are performed by the amplifier/gain adjusting circuits.

4.139 Assuming the 1260A ON HOOK/OFF HK + DIAL/CONT switch is set to the ON HOOK position, ground is applied to level converter Q1 through CR1 and R29. This cuts off Q1 and C5 will now charge to + 12 V through R31 and R14. During this time one-shot U1A is in a stable state with its Q output high. With both inputs of U2A high, Q6 is cut off and Q4 is pinched off by the negative voltage applied through R58 and CR5. The gain of amplifier U4A is now determined by R60 and R61. During pulsing, S21 on the 1260A is set to either the OFF HK + DIAL or the CONT position. The level converter input is now pulled high through a U29 resistor located on A6 in the 1260A. This turns on Q1 and grounds one input of U2A. The resulting low output of U2B turns on Q6 to reverse bias CR5. The 12-dB pad switch turns on and grounds the parallel combination of R42 and R50. These are the gain-setting resistors for U4A and are scaled so that the stage gain is increased by 12 dB. Thus the pulsing level is 12 dB higher than the on-hook level.

4.140 When SF augmentation is desired, switch section S1-3 is opened allowing the reset input of one-shot U1A to be pulled high. This is the normal operating state and the one-shot will be triggered by a positive transition on its A input. Now when S21 is moved to the ON HOOK position, the applied ground will turn off Q1. The resultant positive transition triggers U1A and its Q output goes low for a period of 400 milliseconds. This turns on Q4 increasing the gain of U4A by 12 dB for this period of time and results in an on-hook augmented SF level.

4.141 When sending toward the drop, S2 is set to the SEND-RCV DROP position. The negative voltage applied through R53 and CR4 pinches off Q5 and the pad is disabled. The SF level present at the output of U4A is applied to U4B, which buffers the signal and matches the low impedence of output transformer T2. When S2 is set to the SEND-RCV LINE position, a positive voltage reverse biases CR4 and Q5 is turned on applying ground to R5. The voltage divider comprised of resistors R54 and R55 attenuates by 23 dB the signal applied to the input of U4B. Thus, all levels sent toward the line are reduced by 23 db.

4.142 The SF output signal is available at SF SEND jack J2 through energized relay K1 when S2 is in either the SEND-RCV LINE or the SEND-RCV DROP position. The unit is protected from line transients by CR10. Resistors R4, R5, R23, and the resistance of transformer T2 set the output impedence at 600 ohms. Capacitor C20 provides dc line blocking.

4.143 SF RECEIVER BLOCK DIAGRAM DESCRIPTION

4.144 See Figure 4—15 for the simplified block diagram of the SF receiver. The receiver is functionally an SF-to-dial pulse converter. The SF signal at the SF RCV jack is first amplified to bring it within the range of the tone detectors. Since SF levels received from the line are 23 dB higher than those received from the drop, the output of the input amplifier is attenuated by 23 dB when receiving from the line. The limiter acts as an AGC circuit producing a fixed-level, hard-limited output for all inputs that fall within the dynamic range of the

receiver. Following limiting, a 2600-Hz bandpass filter passes the signal of interest to the tone detectors. The tone detectors perform the SF-to-dial pulse conversion required by the 1260A. Since the bandpass filter introduces a fixed amount of pulse-width distortion, an opposite amount of distortion is introduced by the pulse width adjuster. At this point, any SF pulsing received has been accurately converted to logic level dc dial pulses. A monitor lamp is provided at this point to indicate when the circuit under test is busy. The 1260A receiver requires a high level dial pulse input. This is supplied by the level converter and isolator. The pulses will now be processed by and the resulting measurements displayed on the 1260A.

4.145 SF RECEIVER DETAILED CIRCUIT DESCRIPTION

4.146 See Figure 6—9 for the functional schematic diagram of the SF receive function. The receive function is basically comprised of an input/amplifier, tone detectors, and an output circuit. Each of these is described separately.

4.147 **Input/Amplifier**

4.148 This includes all circuits from SF RCV jack J3 to the output of voltage follower buffer U6A. SF pulsing to be measured is applied through J3 with dc blocking provided by C19. In the SEND-RCV positions of S2, R3 provides a 600-ohm termination. In the MON position the input is bridged by the high impedance of input transformer T1. Varistor CR5 protects the input from high-voltage line transients. Amplification of the input signal is provided by input amplifier U6B. When S2 is set to receive from the drop, a negative voltage is applied through R53 and CR22 to pinch off Q3. In this case, the output of U6B is not attenuated. On the other hand, when S2 is set to receive from the line, CR22 is reverse biased by the positive voltage applied through the switch and Q3 is turned on. This places R53 in the output circuit of U6B and, with R46, causes a 23-dB attenuation. This compensates for the 23-dB higher SF level received from the line.

4.149 A type of AGC (Automatic Gain Control) is provided by hard limiter U2A. Resistors R16 and R17 provide a receiver threshold voltage at the limiter so that receiver low level sensitivity can be set. Any input above the threshold causes a hard-limited signal at the output of U6A. Thus, for the full dynamic range of the receiver input, a constant-amplitude signal is present at the limiter output. The function of voltage follower buffer U6A is to match the input impedance of the bandpass filter that follows.

4.150 **Tone Detectors**

4.151 These include all circuits from the 2600-Hz bandpass filter up to and including pulse width adjuster U2C. The bandpass filter is made up of low pass section U4B and high pass section U4A. The center frequency is calibrated for 2600 Hz by R38 when internal switch section S1-6 is open. In this case, the bandwidth is calibrated for ±30 Hz by R43. When the SF module is to receive other SF frequencies, the bandwidth is widened to cover the range of 1500 to 4000 Hz by closing switch section S1-6. This places R42 in parallel with the series combination of R43 and R44 to increase the bandwidth. When an SF

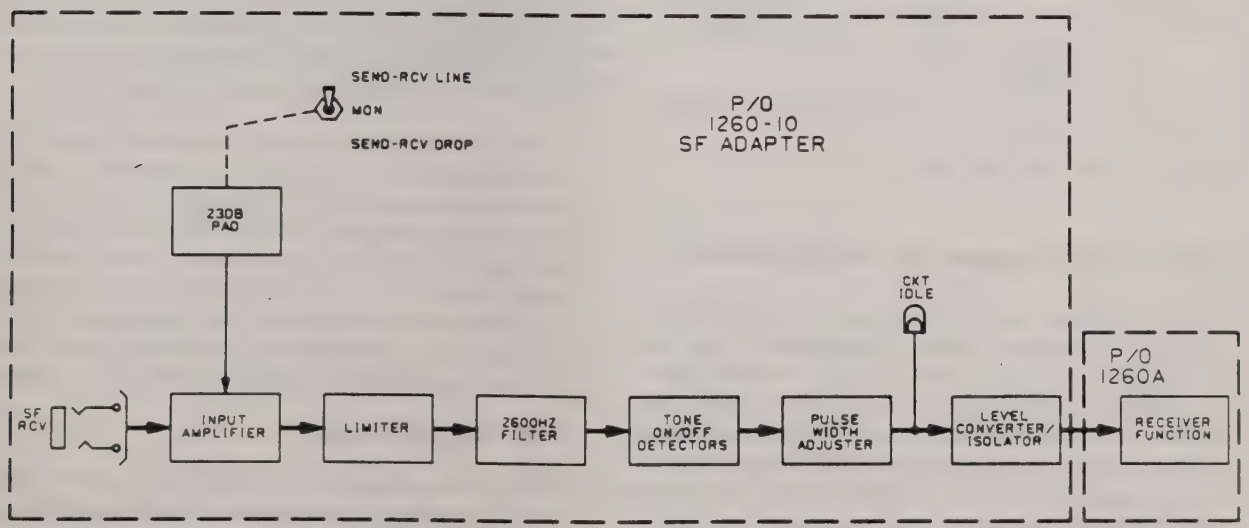


Figure 4—15. SF Receiver Block Diagram.

C 02444-00

tone is first applied to the bandpass filter, the filter response time causes the leading edge of the filter output to be rounded off as illustrated at TP1 on Figure 4—16. In a similar manner, the filter decay time causes rounding of the trailing edge. The narrower the bandwidth the more pronounced the rounding. If this condition is not compensated for, the percent break calculated and displayed by the 1260A will be in error.

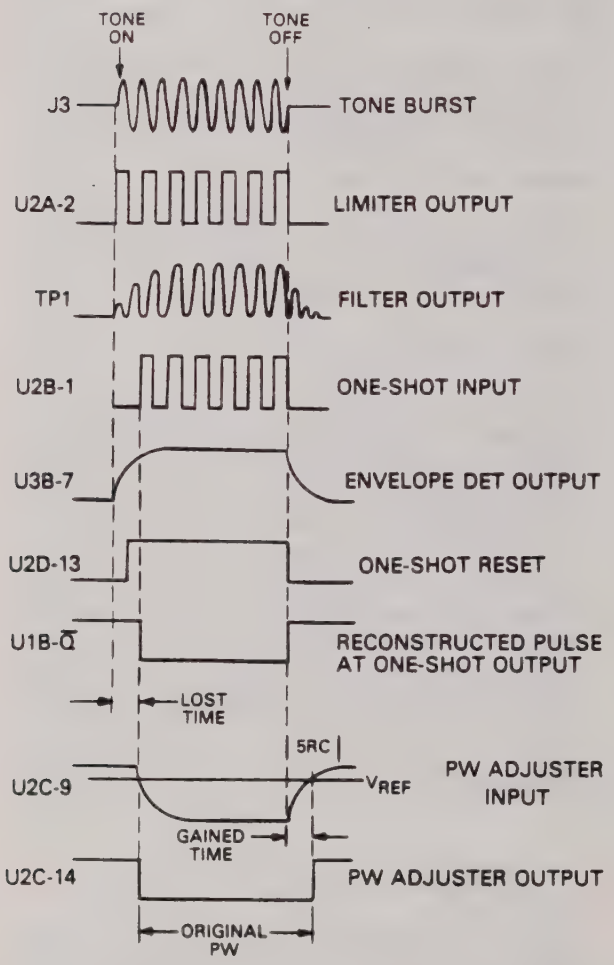


Figure 4—16. SF Receiver Conversion Waveforms.

4.152 The leading and trailing edges of an SF tone are detected by separate circuits. The leading or tone present edge is detected by U2B. During a no-tone condition, R8 and R9 bias the inverting input of U2B positive and the output of this stage is low. The leading edge of the first cycle from the bandpass filter that exceeds the bias voltage on U2B will force the output of this stage high, triggering one-shot U1B. Because of the filter response time, several cycles of the input tone will be required before the threshold of U2B is exceeded. The first pulse to exceed the threshold causes the output of the one-shot to go low. Succeeding cycles of the tone will retrigger the one-shot for the duration of the tone. If the same detector were to be used to detect tone dropout, the reconstructed pulse would be eight milliseconds too long due to the period of the one-shot. For this reason a separate detector is used for tone dropout.

4.153 The combination of U3A and U3B form an envelope detector. The output of the bandpass filter is rectified by U3A and inverted and filtered by U3B. The output of this stage is a positive voltage envelope of the tone. The leading edge of the envelope plays no part in SF detection. While a tone is present, the output of U3B is high. Due to the voltage divider comprised of R13 and R21, the non-inverting input of U2D is more positive than the inverting input. This forces the output high and allows the one-shot to operate in the retrigger mode during tone time. At the instant tone is lost, the output of U3B starts to go low. Capacitor C4, which charged to the output voltage of 43B during tone, prevents the inverting output of 42D from following the output of 43B. The non-inverting input of 42D then quickly becomes negative with respect to the inverting input and the output of U2D goes low, resetting the one-shot. This terminates tone detection.

4.154 The reconstructed pulse at the output of U1B is too short due to leading edge distortion caused by the bandpass filter. Since tone time represents break time, the percent break calculated and displayed by the 1260A will be too low unless pulse width correction is provided. Pulse width adjuster U2C is used to lengthen the pulse break-time by an amount equal to that previously lost in tone detection. As shown on Figure 4—16 the output of one-shot U1B is high during the time the tone is absent. There is enough time between tone bursts for C6 to fully charge to this high level. This level will always be more positive than the threshold level on the inverting input of U2C. This is the idle state of the pulse width adjuster as it waits for the reconstructed pulse to occur.

4.155 The waveform at U2C-9 shown on Figure 4—16 is shaped by the time constant of R18 and C6 when a level change occurs at the output of U1B. By varying the threshold voltage on U2C, the output pulse width can be varied. In the narrow band mode, (2600 Hz) switch section S1-7 is open and R20 adjusts the threshold voltage to compensate for distortion when the filter is in the narrow band mode. In the broad band mode, S1-7 is closed and R27 adjusts the threshold voltage.

4.156 **Output Circuits**

4.157 After obtaining an output from the tone detector it is necessary to alter the level to be compatible with the 1260A receiver. During the time a tone is present at the SF module the output of U2C will be low. This lights CKT IDLE indicator DS1.

4.158 Current through the LED half of opto isolator U5 causes the photo transistor half to conduct and remove the negative bias voltage from level converter Q2. This cuts off Q2 and the level at TP2 drops to −48 V dc. This is the on-hook level required by the 1260A. During the absence of tone, the opto isolator is cut off and a negative bias is applied to Q2 through R28 and CR13. This turns on Q2 resulting in a ground level at TP2. If a plug has been inserted into J3, the pulse is then sent to the 1260A receiver.

4.159 LOCAL PULSE REPEATING ARTLINE OPTION 1260-12 CIRCUIT DESCRIPTION

4.160 The function of the artline option is to provide a means of inserting balanced loop resistance ahead of the 1260A receiver when receiving either dry loop or wet loop pulsing. See Figure 6−35 for the schematic diagram of the artline option. The tip and ring carried through the 1260A are applied to pins 8 and 7. When the THRU pushbutton is pressed and latched, the inputs are routed directly to output pins J and H, bypassing the loop resistance. When any of the resistance pushbuttons is pressed and latched and when the THRU pushbutton is not latched, one half of the resistance value indicated on the selected pushbutton is placed in a series with the tip and one half in series with the ring. None of the pushbutton switches are mechanically interlocked so that loop resistance, once selected, can be bypassed simply by latching the THRU pushbutton.

4.161 As a reminder that loop resistance has been placed in the receiving path, an indicator is made to flash whenever the THRU pushbutton is not latched. This activates a unijunction transistor relaxation type oscillator. Capacitor C1 alternately charges to the supply voltage and then discharges through Q1 to generate a continuous stream of pulses across R19. These are used to flash DS1.

4.162 MONITOR ADAPTER OPTION 1260-13 CIRCUIT DESCRIPTION

4.163 The function of the monitor adapter is to allow a 1260A operator to establish voice communications with another craftsman so that they can jointly perform the necessary testing. See Figure 6−37 for the schematic diagram of the monitor adapter. Normally, a telephone headset of some type would be plugged into MONITOR jack J1 and a communications line such as an order wire pair plugged into SEND LOOP jack J2. When S1 is set to the SEND LOOP position the tip and ring at pins 5 and 6 of P1 are connected to the transmitter section of the 1260A. If desired, the 1260A can now be used to dial pulse over the communications line connected to J2. After the number has been outpulsed, S1 is set to the MONITOR position to establish voice communications. Resistor R1 provides loop holding and termination.

4.164 AC POWER SUPPLY OPTION 1260-11 CIRCUIT DESCRIPTION

4.165 The function of the ac power supply option is to allow the 1260A to operate from either 115 or 230 V ac. See Figure 6−39 for the schematic diagram of the power supply. The supply is a series regulated type furnishing an output of −48 V dc. Switch S1 can be positioned so that either 115 or 230 V ac can be used as the source voltage. Full wave bridge rectifier CR2 through CR5 generates the raw voltage for the regulator. The regulator reference voltage is set by Zener diode CR1. Error amplifier Q2 compares this with a sample of the output voltage picked off by voltage divider R1, R2, and R3. The error amplifier output adjusts the current through series pass transistor Q1 to maintain a regulated output of −48 V dc.

SECTION 5

CALIBRATION

5.1 This section provides the calibration instructions for the 1260A Pulsing Test Set and the 1260-10 SF Adapter option. Part of the SF Adapter calibration procedure is based on the use of a calibrated 1260A. Before attempting to calibrate the SF Adapter, check the 1260A calibration.

5.2 REQUIRED TEST EQUIPMENT

5.3 Table 5—1 lists the test equipment required to calibrate the 1260A Pulsing Test Set and the 1260-10 SF Adapter. Critical specifications are given to facilitate selection of equivalent test equipment.

5.4 1260A CALIBRATION PROCEDURE

5.5 There are two calibration adjustments in the 1260A. They are the receiver threshold adjustment and the transmitter pulse width adjustment. The receiver is used to calibrate the transmitter and, therefore, must be calibrated first. Follow the procedure exactly as presented.

1. Remove the three screws securing the top cover and remove the cover.

2. Apply – 48 V dc or 115/230 V ac as appropriate to the unit and set the POWER switch to ON.

3. Connect a variable power supply and a digital multimeter to the LOOP RCV jack as shown on Figure 5—1. **The tip must be negative with respect to the ring.**

4. Set the RECEIVE mode switch to WET LOOP and the E&M/LOOP switch to TERM.

5. Set the power supply output voltage to 4.50 V dc.

6. On the analog receiver board, set receiver threshold adjustment R4 fully counterclockwise. See Figure 5—2 for location of this adjustment. The 1260A precent break meter should now be indicating ON HOOK.

7. Slowly adjust R4 clockwise until the front panel meter just jumps to the OFF HOOK position.

8. Remove the variable power supply and the digital multimeter.

9. Using a cord equipped with 310 plugs on each end, insert one end into the LOOP SEND jack and the other into the LOOP RCV jack.

10. Set both the SEND and the RECEIVE mode switches to DRY LOOP, the E&M/LOOP switch to TERM, the ON HOOK/OFF HK + DIAL/CONT switch to CONT, the PPS thumbwheel switches to 20.0, and the % BREAK thumbwheel switches to 60.0. Ensure that all LOOP RES and LINE LEAK pushbuttoms are unlatched.

11. On the leak board, adjust transmitter pulse width adjustment R1 to obtain a % BREAK indication of 60.0 on the front panel display. See Figure 5—2 for the location of this adjustment.

12. Remove the power and replace the top cover.

Table 5—1. Test Equipment Required for Calibration.

EQUIPMENT TYPE	TYPICAL MODEL (OR EQUIVALENT)	CRITICAL SPECIFICATIONS
Variable power supply	–	Output voltage: 4.5 V dc
Digital volt meter	HP 3435A	Accuracy: 1% Digits :3
Audio signal generator	HP 204C	Frequency range: 2500-2700 Hz Level range: –42 to 0 dBM into 600 ohms
Frequency counter	HP 5314A	Frequency: up to 2700 Hz Digits: 5 Accuracy: 0.1%
AC voltmeter	HP 400FL	dB scale: calibrated for 600 ohms Accuracy: 0.5%
Return loss set	Wiltron 9031	Impedance: 600 ohms Frequency: 2600 Hz
Load resistor	–	600 ohms, 1%

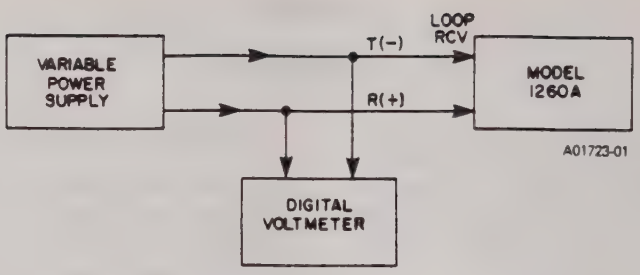


Figure 5—1. Typical Model 1260A Receiver Threshold Calibration Test Setup.

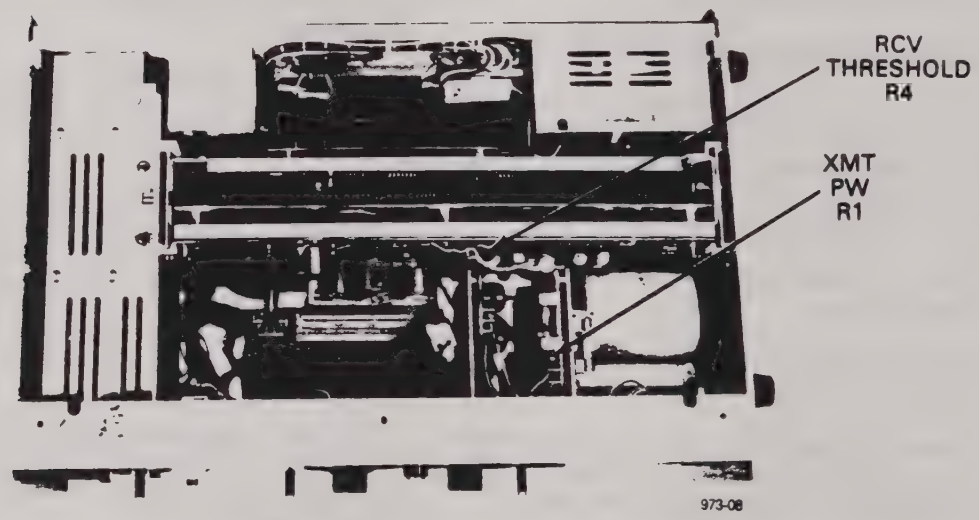


Figure 5—2. 1260A Calibration Adjustment Locations.

5.6 SF ADAPTER OPTION 1260-10 CALIBRATION PROCEDURE

5.7 There are five adjustments in the send section of the SF module and five in the receive section. The send section is used in part to calibrate the receive section and therefore must be calibrated first. In addition, the 1260A is used to calibrate the SF Adapter option and must be checked for calibration before proceeding. An extender board is required to gain access to the calibration adjustments. Follow the procedure exactly as presented.

1. Remove the SF Adapter option from the 1260A.

2. Remove the six screws securing the clear plastic protective shield and remove the shield.

3. Replace the two screws to secure board B to the hinges on board A.

4. Insert an extender board into the empty 1260A slot.

5. Insert the SF option into the extender board.

6. Swing board B down as far as it will go without putting excessive strain on the connector joining board B and the wire harness. This will give complete access to all calibration adjustments.

7. Apply − 48 V dc or 115/230 V ac as appropriate to the 1260A and set the POWER switch to ON.

8. On board B, set DIP switch section S1-1 and S1-2 to ON and section S1-6 and S1-7 to OFF. See Figure 5—3 for location of S1.

9. Connect a frequency counter to TP1 on board B. See Figure 5—4.

10. The frequency counter indication should be within the range of 2595 to 2605 Hz. If it is not, adjust R15 on board B for an indication of 2600 Hz.

11. On board B, set DIP switch sections S1 – 1 and S1 – 2 to OFF.

12. The frequency counter indication should be within the range of 2395 to 2405 Hz. If it is not, adjust R1 on board B for an indication of 2400 Hz.

13. Remove the frequency counter.

14. Ground the output end of C8. See Figure 5 – 4.

15. Set the LINE/MON/DROP switch to either SEND-RCV LINE OR SEND-RCV DROP.

16. Connect a return loss measuring set to the SF SEND jack.

17. Set up the return loss measuring set frequency for 2600 Hz and set the test impedance to 600 ohms.

18. The return loss measured should be greater than 25 dB. If it is not, adjust R4 on board A for maximum return loss.

19. Remove the short to ground on C8.

20. Connect a 600-ohm 1% load resistor between the tip and ring of a 310 plug.

21. Insert the plug and load resistor into the SF SEND jack and connect an ac voltmeter across the resistor.

22. On board B, set DIP switch sections S1 – 1 and S1 – 2 to ON.

23. On the 1260A, set the ON HOOK/OFF HK + DIAL/CONT switch to ON HOOK and the SEND and RECEIVE mode switches to E(SF)G&B.

24. Set the DEV FR SND TLP switch to 0 dB and the LINE/MON/DROP switch to SEND-RCV DROP.

25. The ac voltmeter indication should be within the range of – 12.5 to – 13.5 dBm. If it is not, adjust R51 on board B for an indication of – 13 dBm.

26. Connect an audio oscillator and ac voltmeter to the EXT OSC jack.

27. Set the oscillator frequency to 2600 Hz and the output level to 0 dBm as indicated on the voltmeter.

28. Connect the ac voltmeter across the load resistor at the SF SEND jack.

29. The ac voltmeter indication should be within the range of – 12.5 to – 13.5 dBm. If it is not, adjust R8 on board B for an indication of – 13 dBm.

30. Connect an audio oscillator, ac voltmeter, and frequency counter to the SF RCV jack.

31. Set the oscillator frequency to 2600 Hz and the output level for – dBm at the SF RCV jack.

32. Connect the ac voltmeter to TP1 on board A. See Figure 5 – 4.

33. On board A, set R16 fully counterclockwise and R43 fully clockwise.

34. Set the LINE/MON/DROP switch to SEND-RCV LINE.

35. On board A, adjust R38 to obtain a maximum indication on the ac voltmeter.

36. Set the oscillator frequency to 2675 Hz.

37. On board A, adjust R43 counterclockwise until the 1260A percent break meter just jumps to the OFF HOOK indication.

38. Slowly decrease the oscillator frequency until the 1260A front panel meter drops back to ON HOOK and continue to decrease the frequency until the meter again jumps to OFF HOOK.

39. The frequency counter indication should be within the range of 2520 to 2530 Hz.

40. If the frequency indicated in step 39 was too high, repeat steps 36 through 39 using a starting frequency in step 36 that is lower than the original 2675 Hz. If, on the other hand, the frequency was too low, use a starting frequency that is higher than 2675 Hz. The calibration is correct when the upper frequency of the bandwidth is within the range of 2670 to 2680 Hz and the lower frequency within the range of 2520 to 2530 Hz.

NOTE

When repeating step 36, always start by turning R43 fully clockwise, then make the adjustment

41. Set the LINE/MON/DROP switch to MON

42. With the oscillator, ac voltmeter, and frequency counter connected to the SF RCV jack, set the oscillator frequency to 2600 Hz and the output level to – 42 dBm at the SF RCV jack.

43. On board A, slowly adjust R16 clockwise until the 1260A front panel meter jumps to the OFF HOOK position.

44. Remove all test equipment from the SF Adapter.

45. Using a cord equipped with 310 plugs on each end, insert one end into the SF SEND jack and the other into the SF RCV jack.

46. Set the DEV FR SND TLP switch to 0 dB and the LINE/MON/DROP switch to SEND-RCV DROP.

47. Set the 1260A ON HOOK/OFF HK + DIAL/CONT switch to CONT, the PPS thumbwheel switches to 14.0, the % BREAK thumbwheel switches to 75.0, and the SEND and RECEIVE mode switches to E(SF) G&B.

48. On board A, adjust R20 to obtain a 1260A % BREAK display of 75.0.

49. On board B, set DIP switch sections S1-6 and S1-7 to ON.

50. On board B, adjust R27 to obtain a 1260A % BREAK indication of 75.0. This completes the receiver section calibration.

51. Remove all test equipment, install the clear plastic shield, and insert the SF Adapter into the 1260A slot.

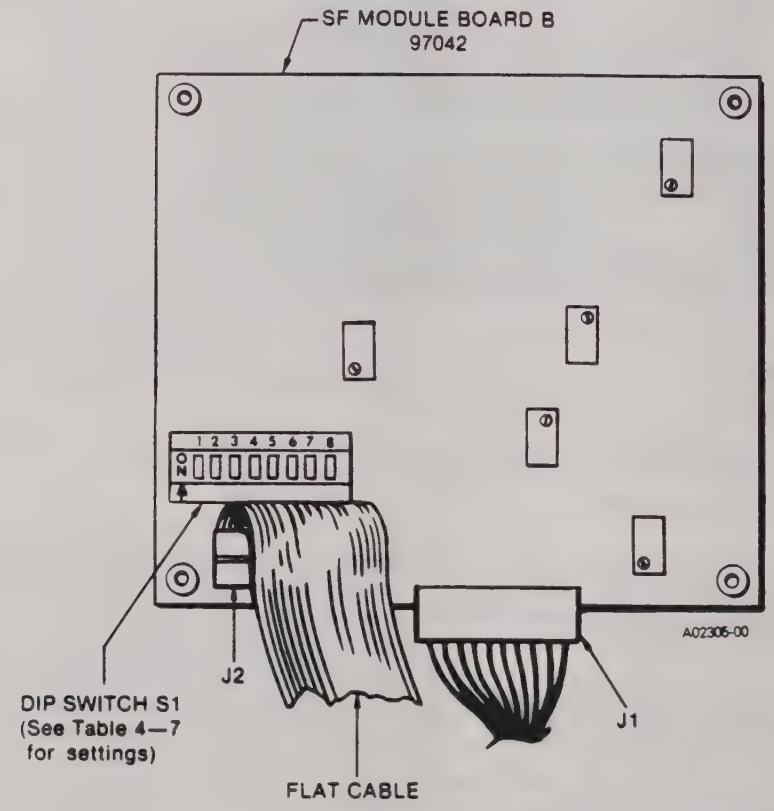


Figure 5–3. SF Adapter Board B DIP Switch S1 Location.

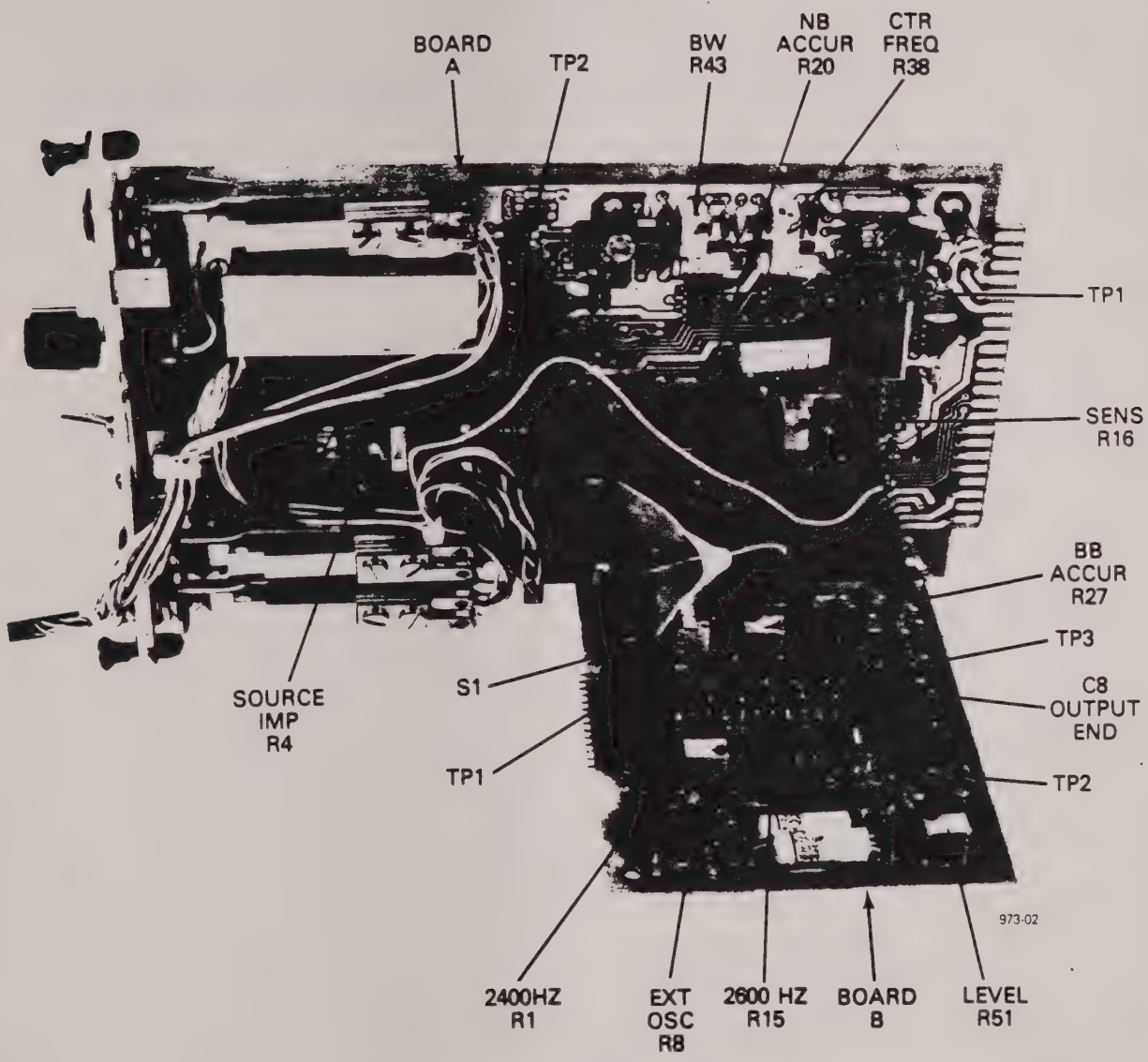


Figure 5—4. SF Adapter Calibration Adjustment Locations.

SECTION 6

DIAGRAMS

6.1 This section contains functional, parts location, and schematic diagrams for the Model 1260A.

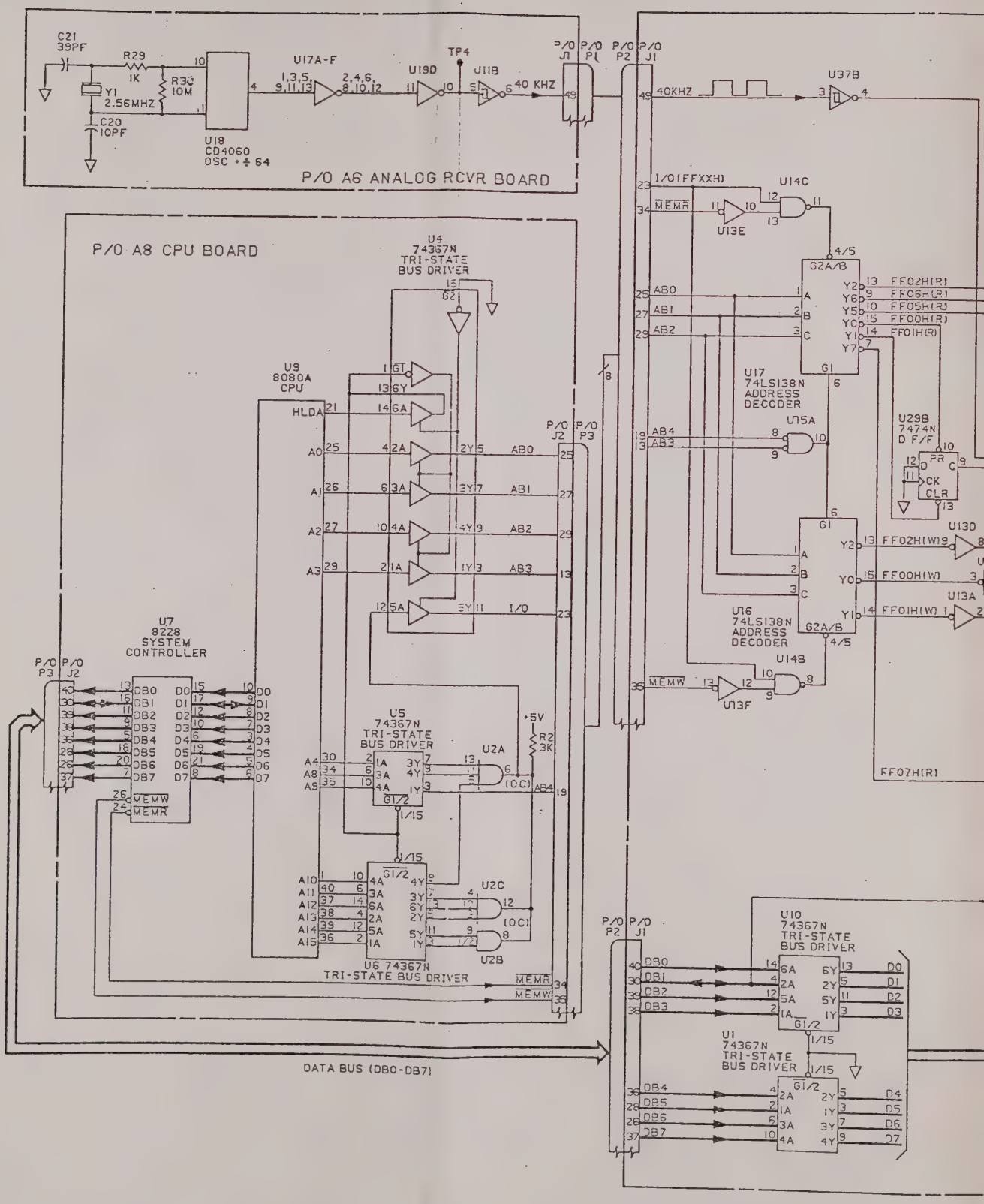
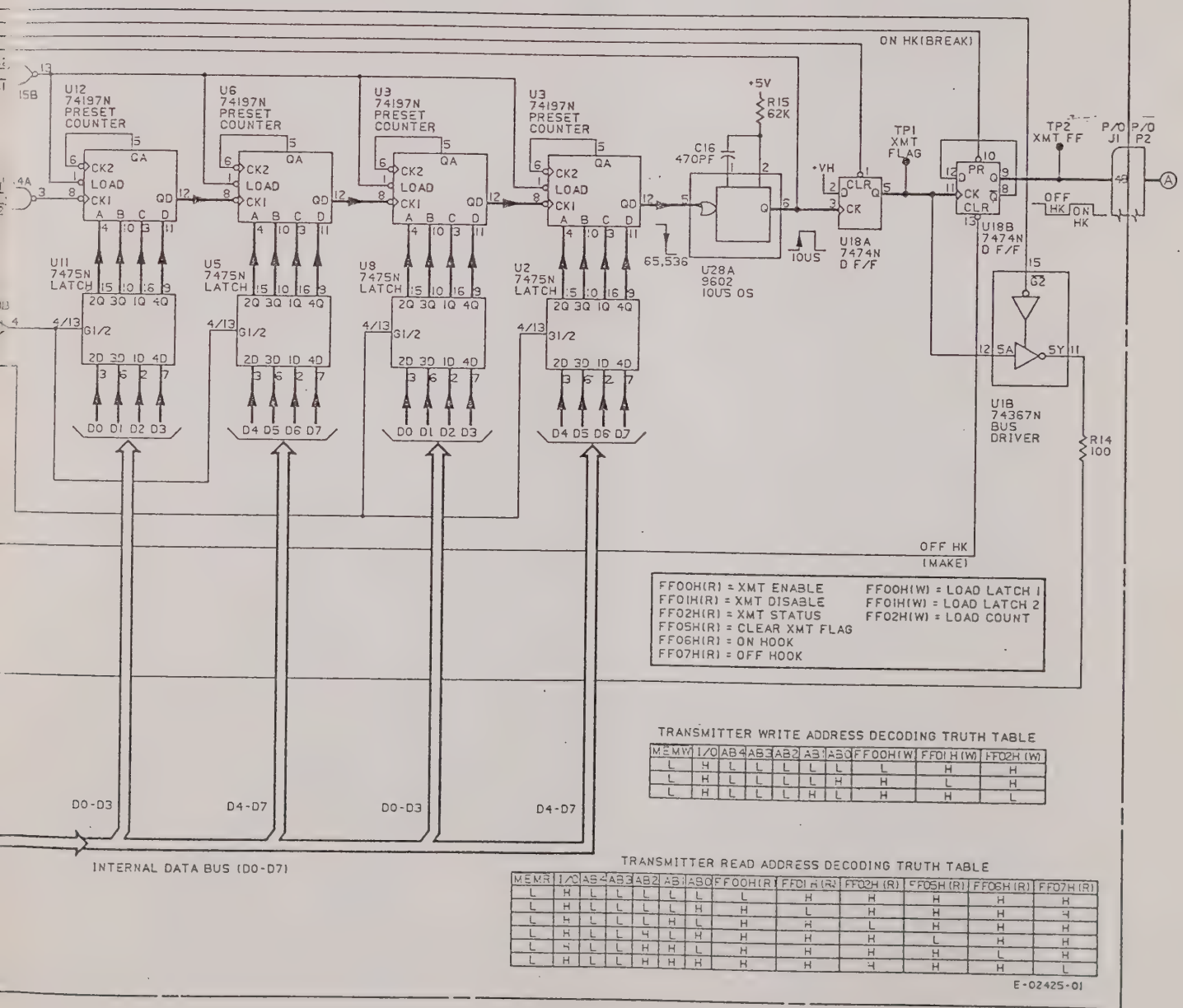


Figure 6—1. Transmitter Functional Schematic Diagram. (Sheet 1 of 2)

P/O A7 XMTR, RCVR + INTFC BOARD



TRANSMITTER WRITE ADDRESS DECODING TRUTH TABLE

MEMW	I/O	AB4	AB3	AB2	AB1	AB0	FF00H(W)	FF01H(W)	FF02H(W)
L	H	L	L	L	L	L	L	H	H
L	H	L	L	L	L	H	H	L	H
L	H	L	L	L	H	L	H	H	L

TRANSMITTER READ ADDRESS DECODING TRUTH TABLE

MEMR	I/O	AB4	AB3	AB2	AB1	AB0	FF00H(R)	FF01H(R)	FF02H(R)	FF05H(R)	FF06H(R)	FF07H(R)
L	H	L	L	L	L	L	L	H	H	H	H	H
L	H	L	L	L	L	H	H	L	H	H	H	H
L	H	L	L	L	H	L	H	H	L	H	H	H
L	H	L	L	H	L	L	H	H	H	L	H	H
L	H	L	L	H	H	L	H	H	H	H	L	H
L	H	L	L	H	H	H	H	H	H	H	H	L

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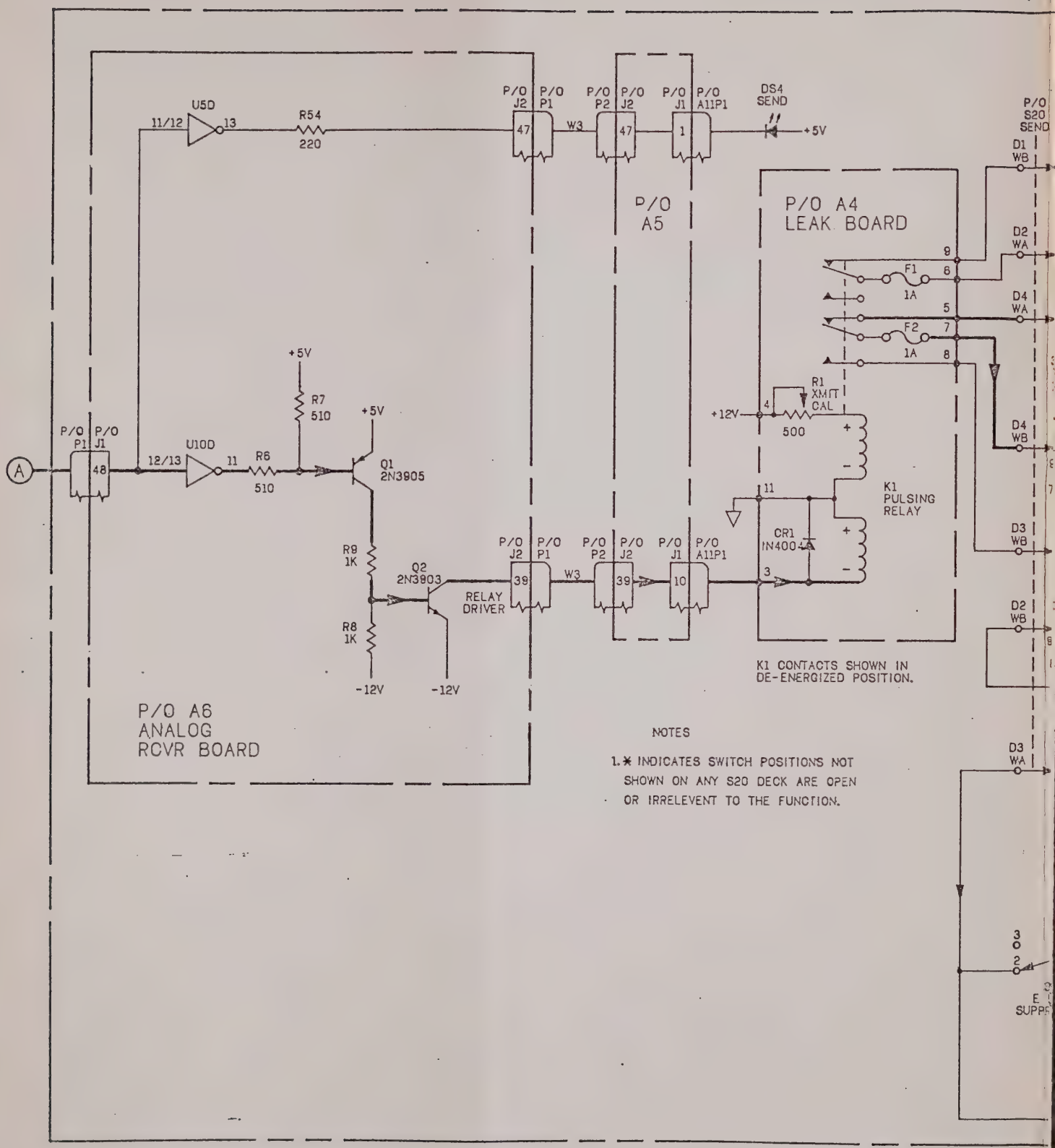

U5D
11/12
13
R54
220
P/O J2
P/O P1
P/O P2
P/O J2
P/O J1
P/O A11P1
47
W3
47
1
DS4 SEND
+5V
P/O S20 SEND
D1 WB
P/O A5
P/O A4 LEAK BOARD
D2 WA
9
F1
1A
6
D4 WA
5
F2
1A
7
8
D4 WB
D2 WB
D3 WB
D3 WA
+5V
R7
510
+5V
R1 XMIT CAL
+12V
4
500
P/O P1
P/O J1
48
A
12/13
U10D
11
R6
510
Q1
2N3905
11
K1 PULSING RELAY
CR1
IN4004
3
R9
1K
Q2
2N3903
R8
1K
RELAY DRIVER
39
W3
39
10
-12V
-12V
K1 CONTACTS SHOWN IN DE-ENERGIZED POSITION.
P/O A6
ANALOG
RCVR BOARD
NOTES
1. * INDICATES SWITCH POSITIONS NOT SHOWN ON ANY S20 DECK ARE OPEN OR IRRELEVENT TO THE FUNCTION.
3
2
E
SUPP

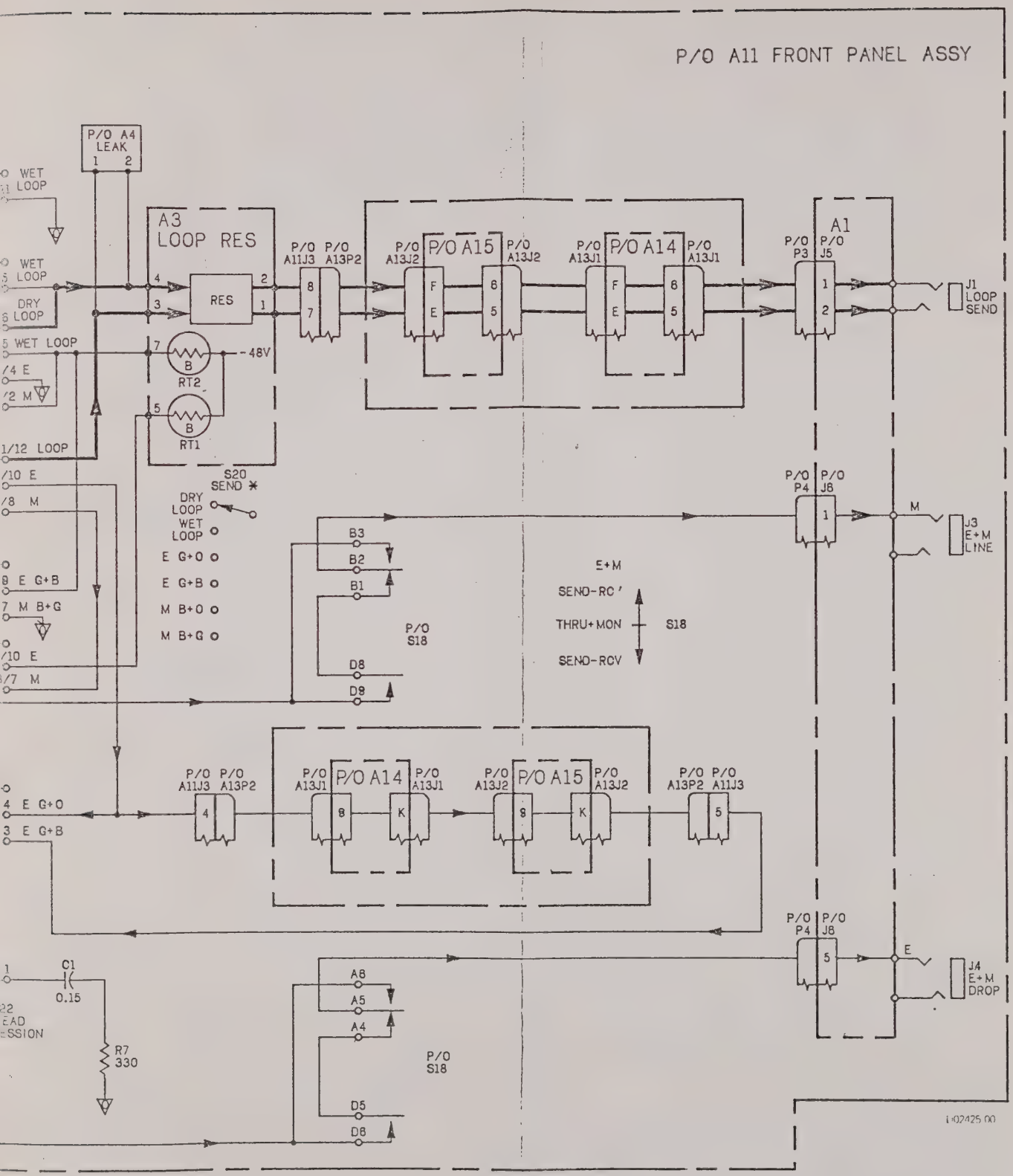
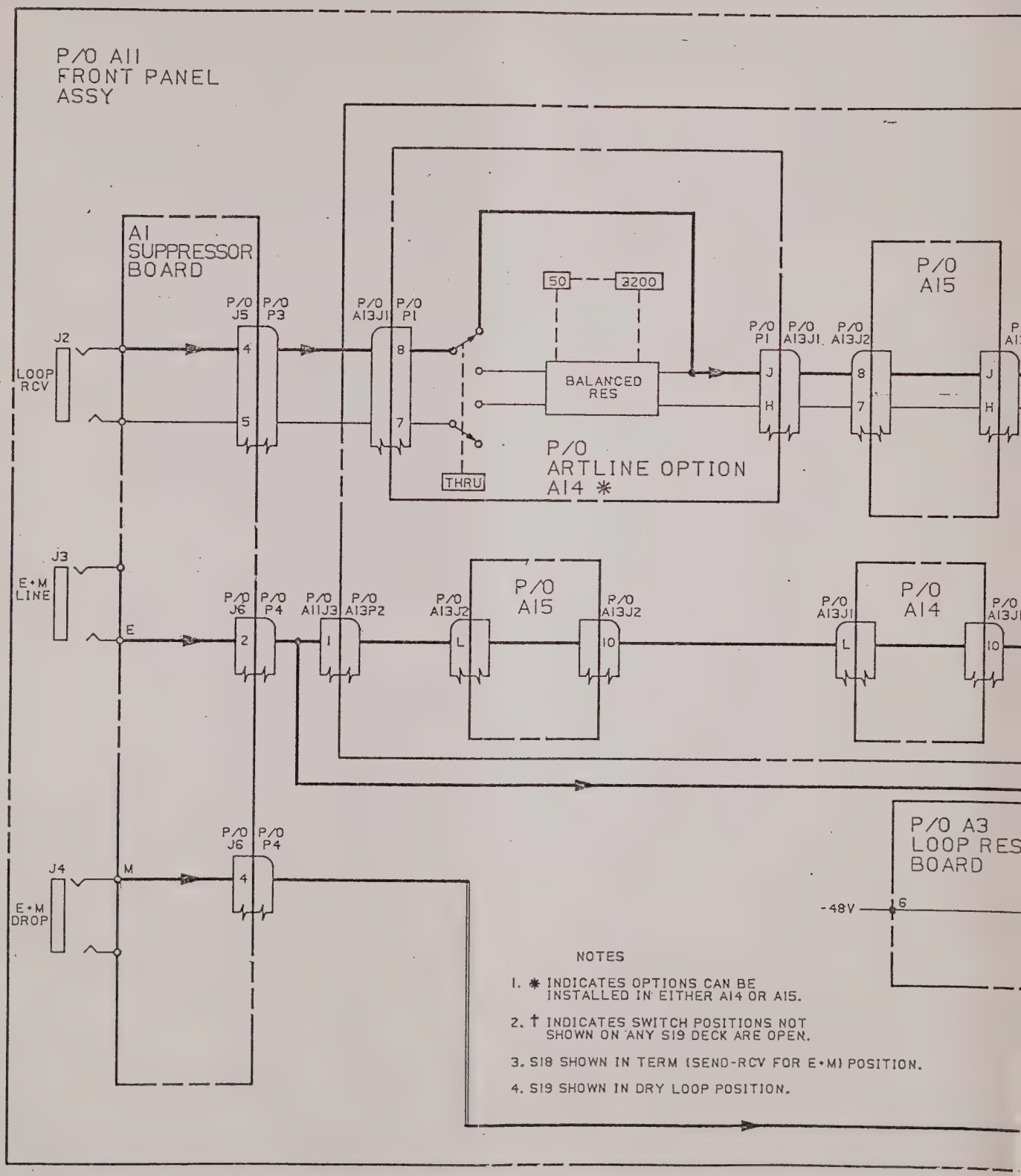


Figure 6—1. Transmitter Functional Schematic Diagram. (Sheet 2 of 2)


P/O A11
FRONT PANEL
ASSY
A1
SUPPRESSOR
BOARD
J2
LOOP
RCV
J3
E+M
LINE
J4
E+M
DROP
P/O J5
P/O P3
P/O J6
P/O P4
P/O A11J3
P/O A13P2
P/O A13J1
P/O P1
P/O A13J2
50
3200
BALANCED
RES
THRU
P/O
ARTLINE OPTION
A14 *
P/O
A15
P/O
A14
P/O A3
LOOP RES
BOARD
-48V
NOTES
1. * INDICATES OPTIONS CAN BE INSTALLED IN EITHER A14 OR A15.
2. † INDICATES SWITCH POSITIONS NOT SHOWN ON ANY S19 DECK ARE OPEN.
3. S18 SHOWN IN TERM (SEND-RCV FOR E+M) POSITION.
4. S19 SHOWN IN DRY LOOP POSITION.

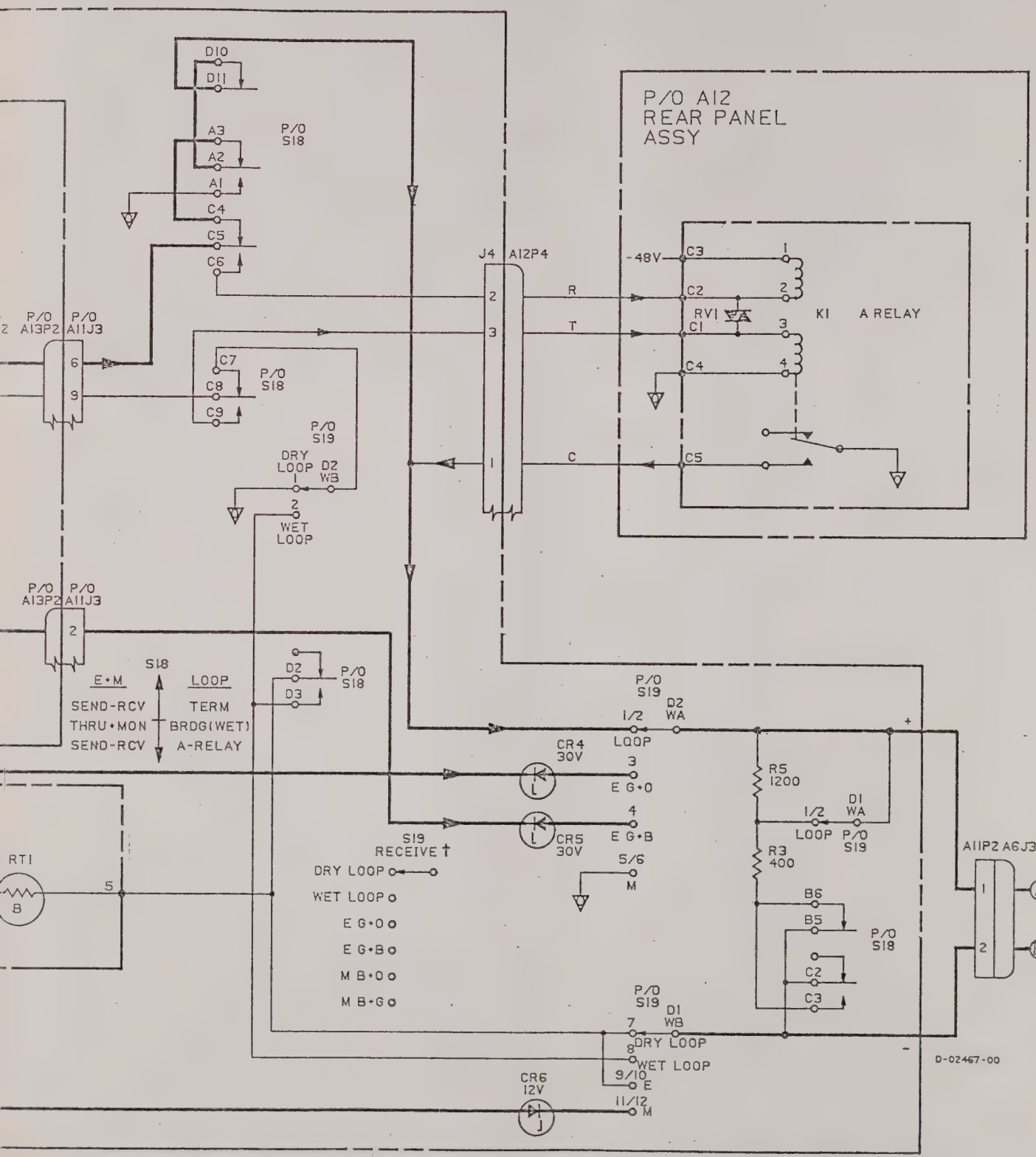
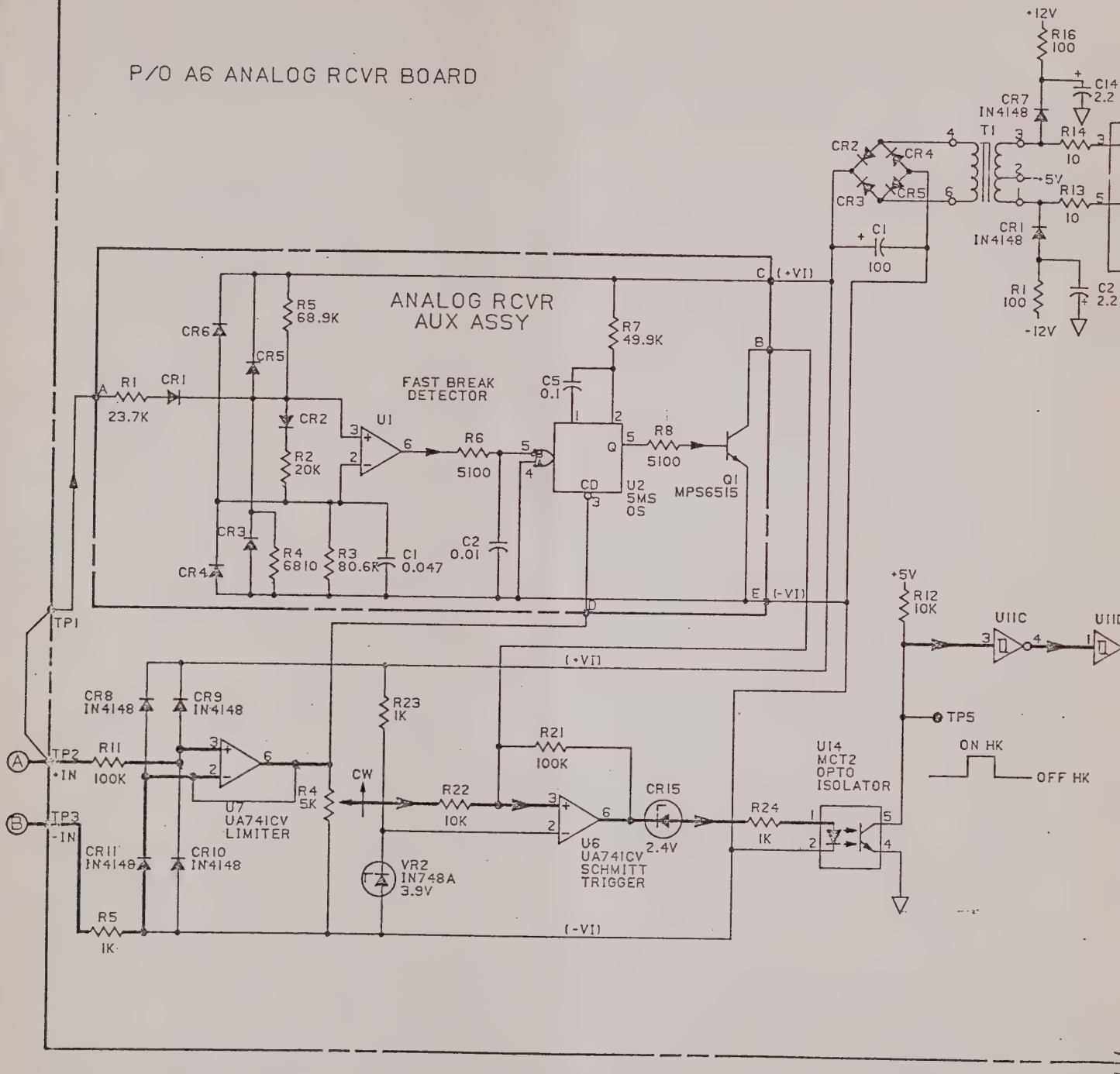


Figure 6—2. Receiver Functional Schematic Diagram. (Sheet 1 of 3)



NOTES

1. UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE IN OHMS, ALL CAPACITORS ARE IN MICROFARADS.
2. ⏚ IS LOGIC GROUND AND ⏚ IS OFFICE GROUND.

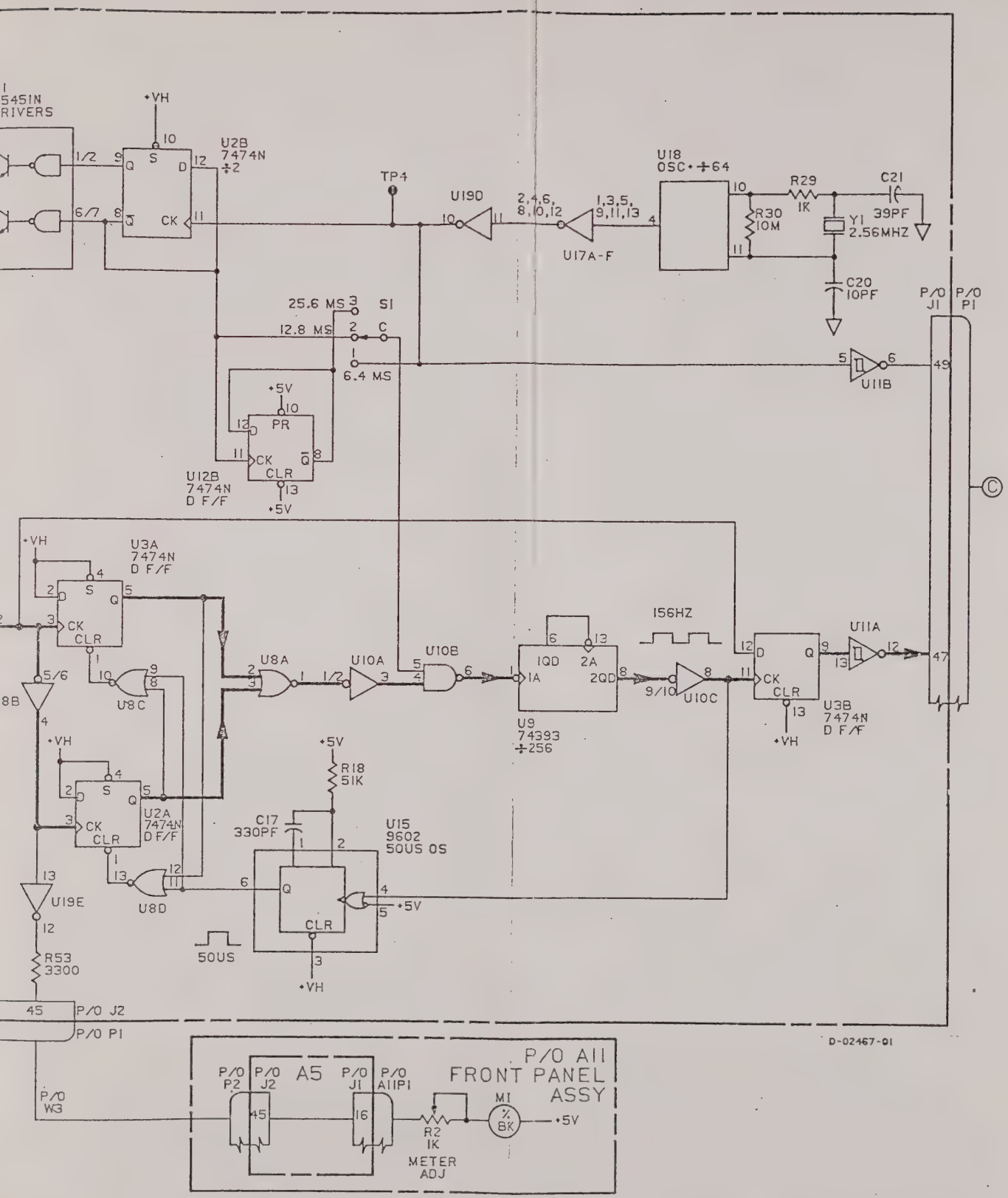
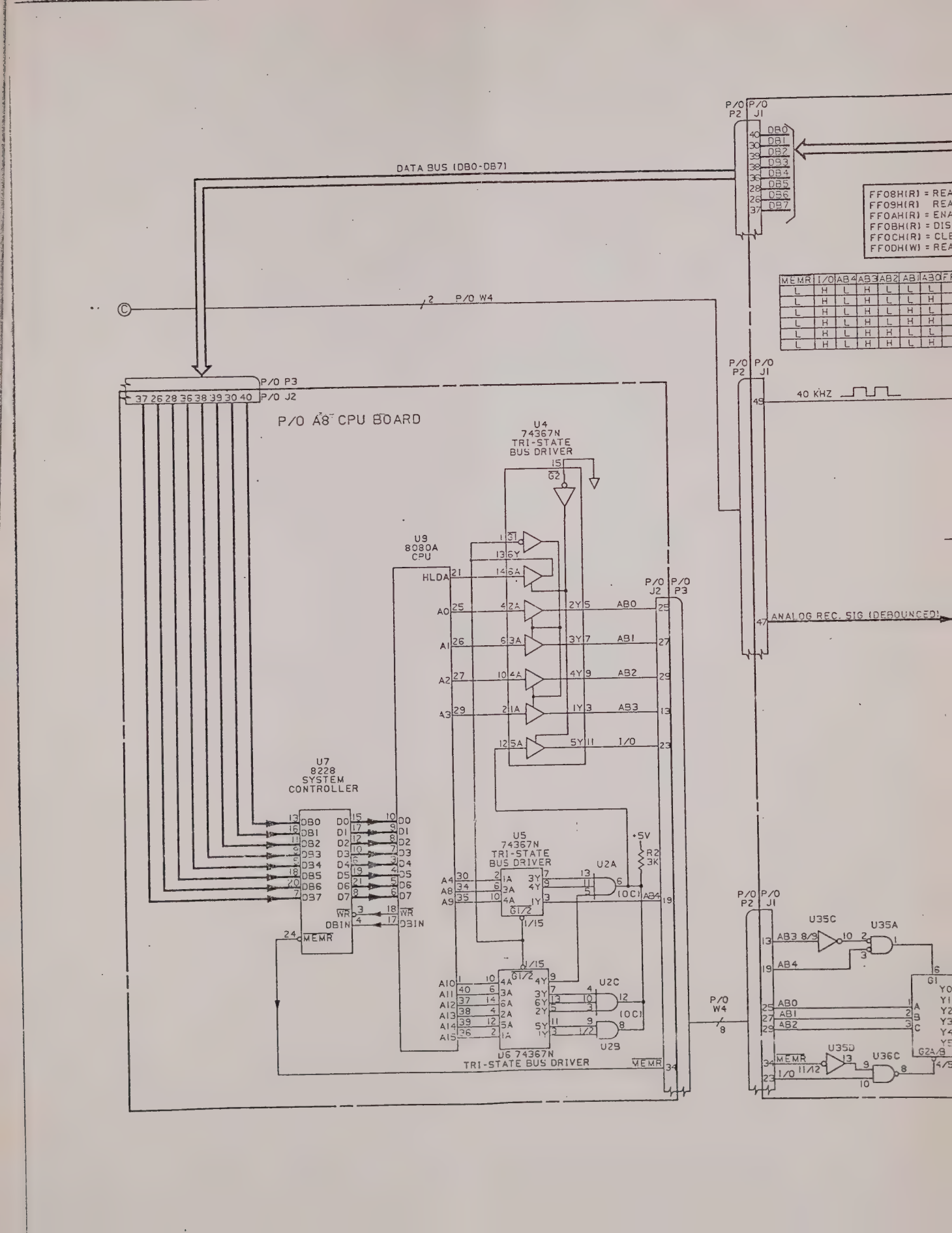


Figure 6—2. Receiver Functional Schematic Diagram. (Sheet 2 of 3)


P/O P2 P/O J1
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DATA BUS (DB0-DB7)
FF08H(R) = REA
FF09H(R) REA
FF0AH(R) = ENA
FF0BH(R) = DIS
FF0CH(R) = CLE
FF0DH(W) = REA
MEMR I/O AB4 AB3 AB2 AB1 AB0
P/O W4
P/O P3
37 26 28 36 38 39 30 40 P/O J2
P/O A8 CPU BOARD
40 KHZ
ANALOG REC. SIG (DEBOUNCED)
U4
74367N
TRI-STATE
BUS DRIVER
U9
8080A
CPU
HLDA
A0
A1
A2
A3
AB0
AB1
AB2
AB3
I/O
U7
8228
SYSTEM
CONTROLLER
DBIN
MEMR
U5
74367N
TRI-STATE
BUS DRIVER
+5V
R2
3K
U2A
U2B
U2C
A4
A8
A9
AB4
A10
A11
A12
A13
A14
A15
U6 74367N
TRI-STATE BUS DRIVER
U35A
U35B
U35C
U35D
AB3 8/9
AB4
AB0
AB1
AB2
MEMR
I/O

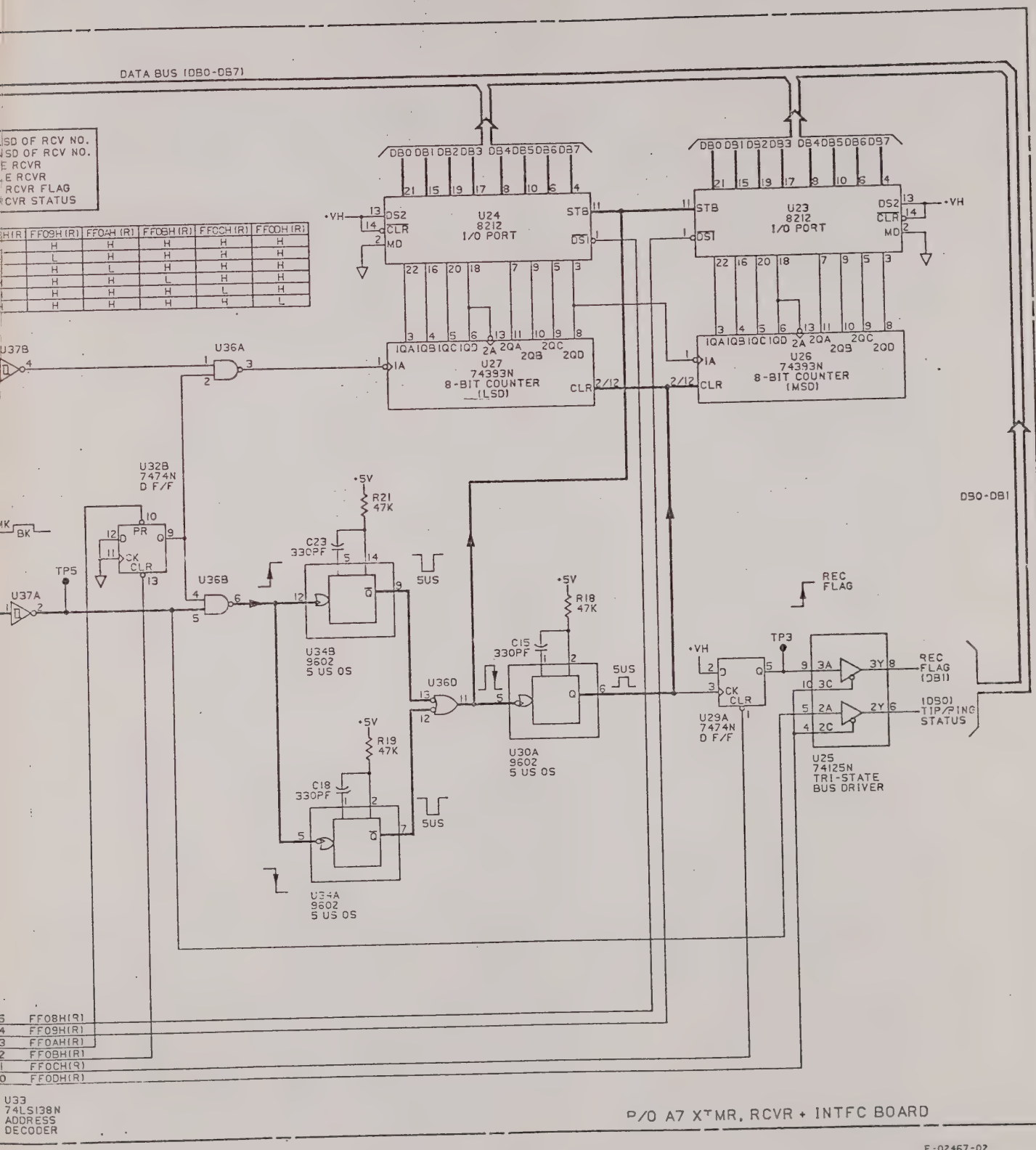
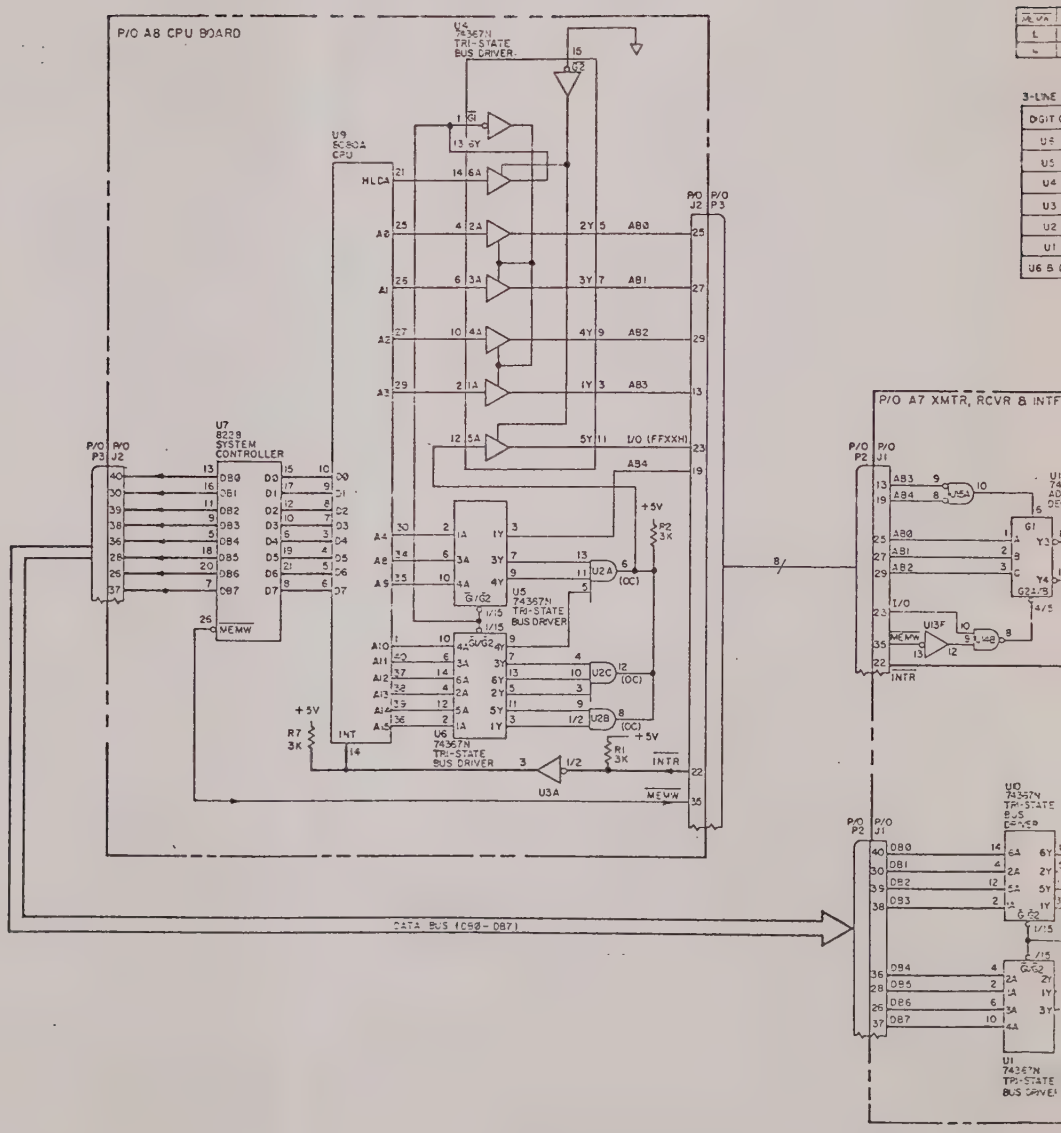


Figure 6—2. Receiver Functional Schematic Diagram. (Sheet 3 of 3)


P/O A8 CPU BOARD
U4
74367N
TRI-STATE
BUS DRIVER.
U9
8080A
CPU
HLDA
A0
A1
A2
A3
AB0
AB1
AB2
AB3
I/O (FFXXH)
AB4
P/O J2
P/O J3
U7
8228
SYSTEM
CONTROLLER
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
MEMW
INT
INTR
+5V
R7
3K
R1
3K
P2
3K
U5
74367N
TRI-STATE
BUS DRIVER
U6
74367N
TRI-STATE
BUS DRIVER
U3A
U2A
U2B
U2C
(OC)
A4
A8
A9
A10
A11
A12
A13
A14
A15
8/
DATA BUS (D80 - D87)
P/O A7 XMTR, RCVR & INTF
P/O P2
P/O J1
U3F
I/O
INTR
U0
74367N
TRI-STATE
BUS DRIVER
U1
74367N
TRI-STATE
BUS DRIVER

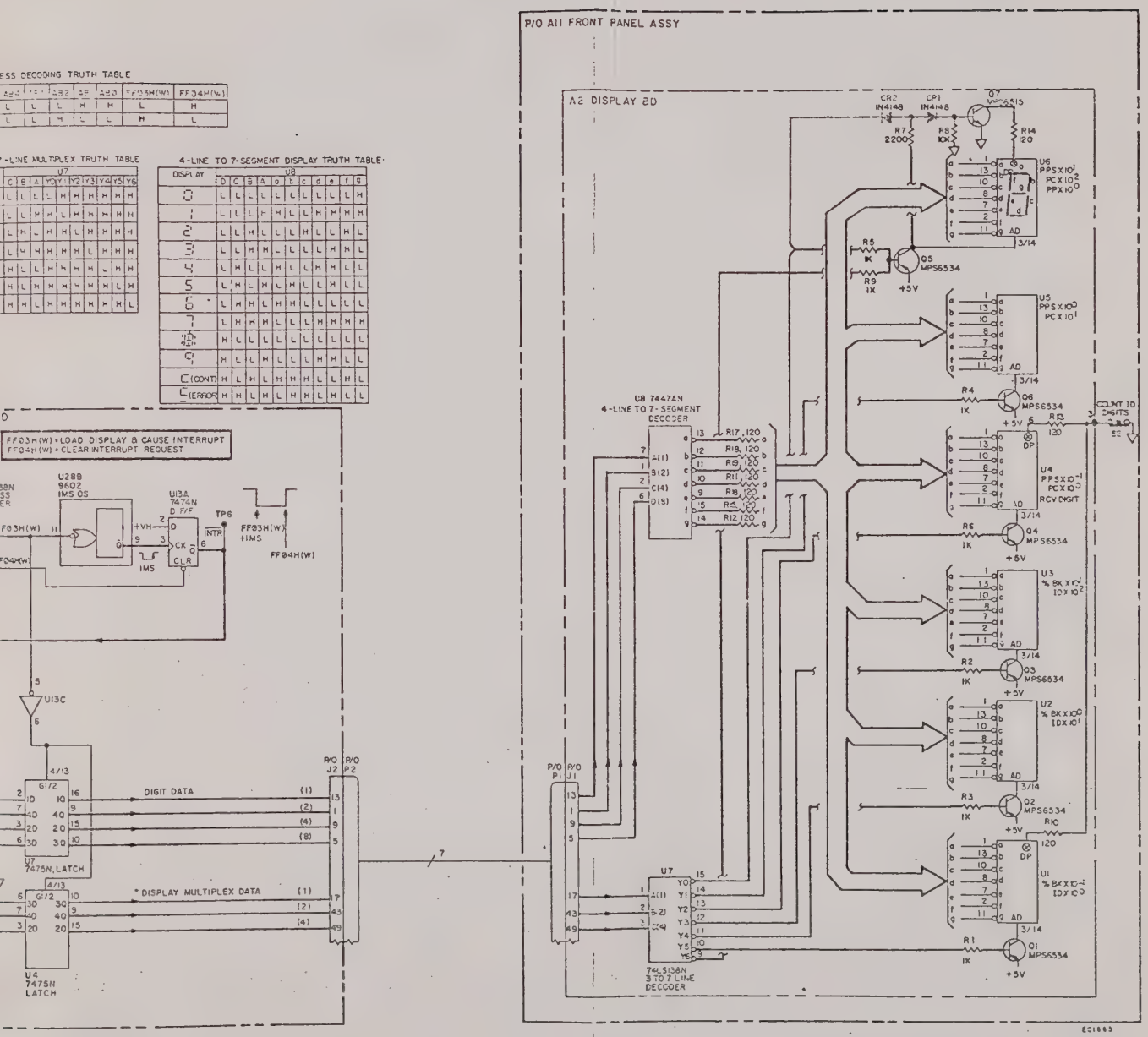
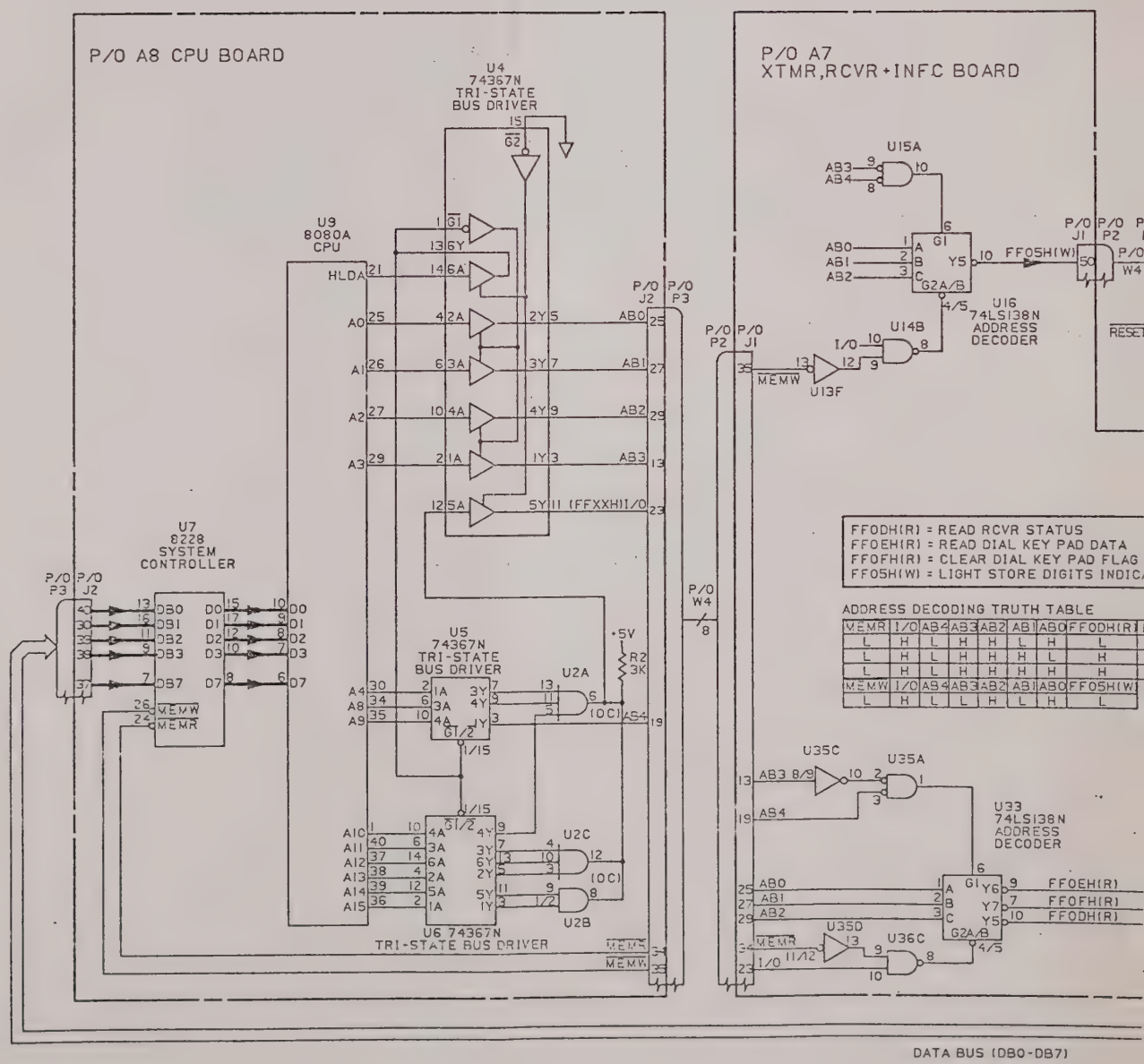


Figure 6—3. Interrupt And Display Functional Schematic Diagram.


P/O A8 CPU BOARD
P/O A7
XTMR,RCVR+INFC BOARD
U4
74367N
TRI-STATE
BUS DRIVER
U9
8080A
CPU
HLDA
A0
A1
A2
A3
AB0
AB1
AB2
AB3
5Y 11 (FFXXH)I/O
U7
8228
SYSTEM
CONTROLLER
DB0
DB1
DB2
DB3
DB7
D0
D1
D2
D3
D7
MEMW
MEMR
U5
74367N
TRI-STATE
BUS DRIVER
A4
A8
A9
AB4
U2A
U2C
U2B
(OC)
+5V
R2
3K
A10
A11
A12
A13
A14
A15
U6 74367N
TRI-STATE BUS DRIVER
U15A
AB3
AB4
AB0
AB1
AB2
FF05H(W)
U16
74LS138N
ADDRESS
DECODER
U14B
I/O
MEMW
U13F
RESET
FF0DH(R) = READ RCVR STATUS
FF0EH(R) = READ DIAL KEY PAD DATA
FF0FH(R) = CLEAR DIAL KEY PAD FLAG
FF05H(W) = LIGHT STORE DIGITS INDIC
ADDRESS DECODING TRUTH TABLE
MEMR I/O AB4 AB3 AB2 AB1 AB0 FF0DH(R)
L H L H H L H L
L H L H H H L H
L H L H H H H H
MEMW I/O AB4 AB3 AB2 AB1 AB0 FF05H(W)
L H L L H L H L
U35C
U35A
AB3 8/9
AB4
U33
74LS138N
ADDRESS
DECODER
FF0EH(R)
FF0FH(R)
FF0DH(R)
U35D
U36C
DATA BUS (DB0-DB7)

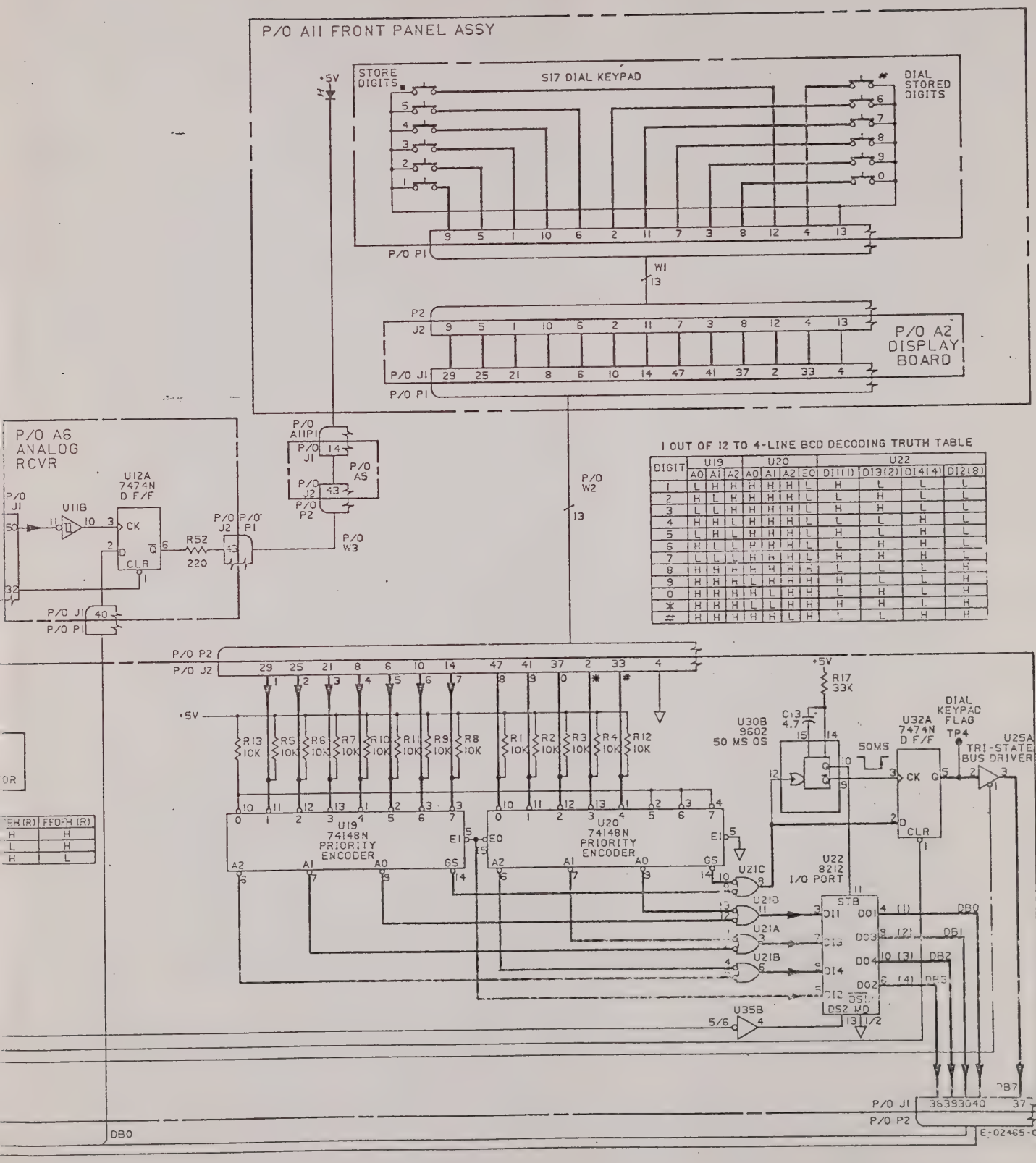


Figure 6—4. Dial Keypad Data Entry Functional Schematic Diagram.

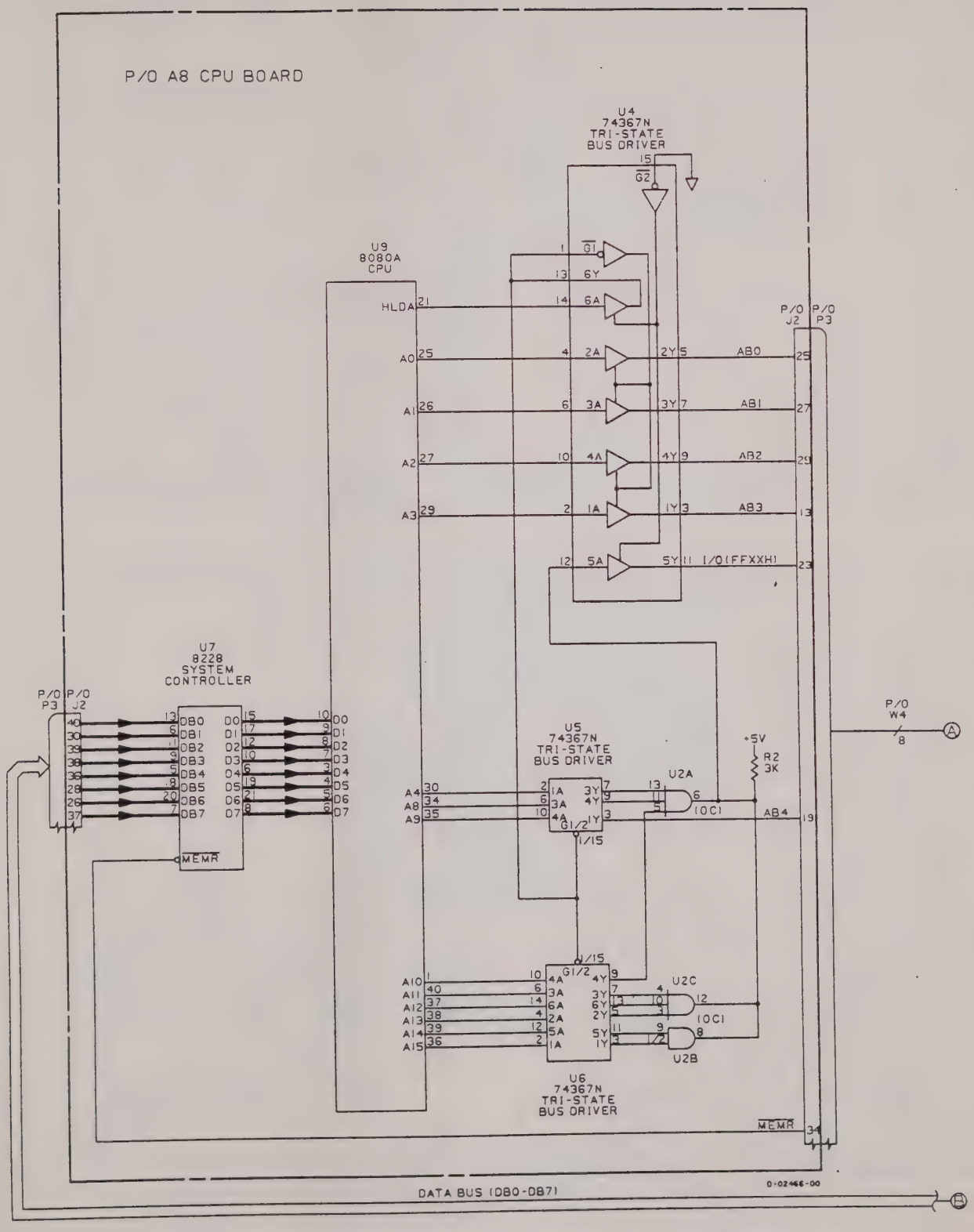


Figure 6—5. Switch Status Functional Schematic Diagram. (Sheet 1 of 2)

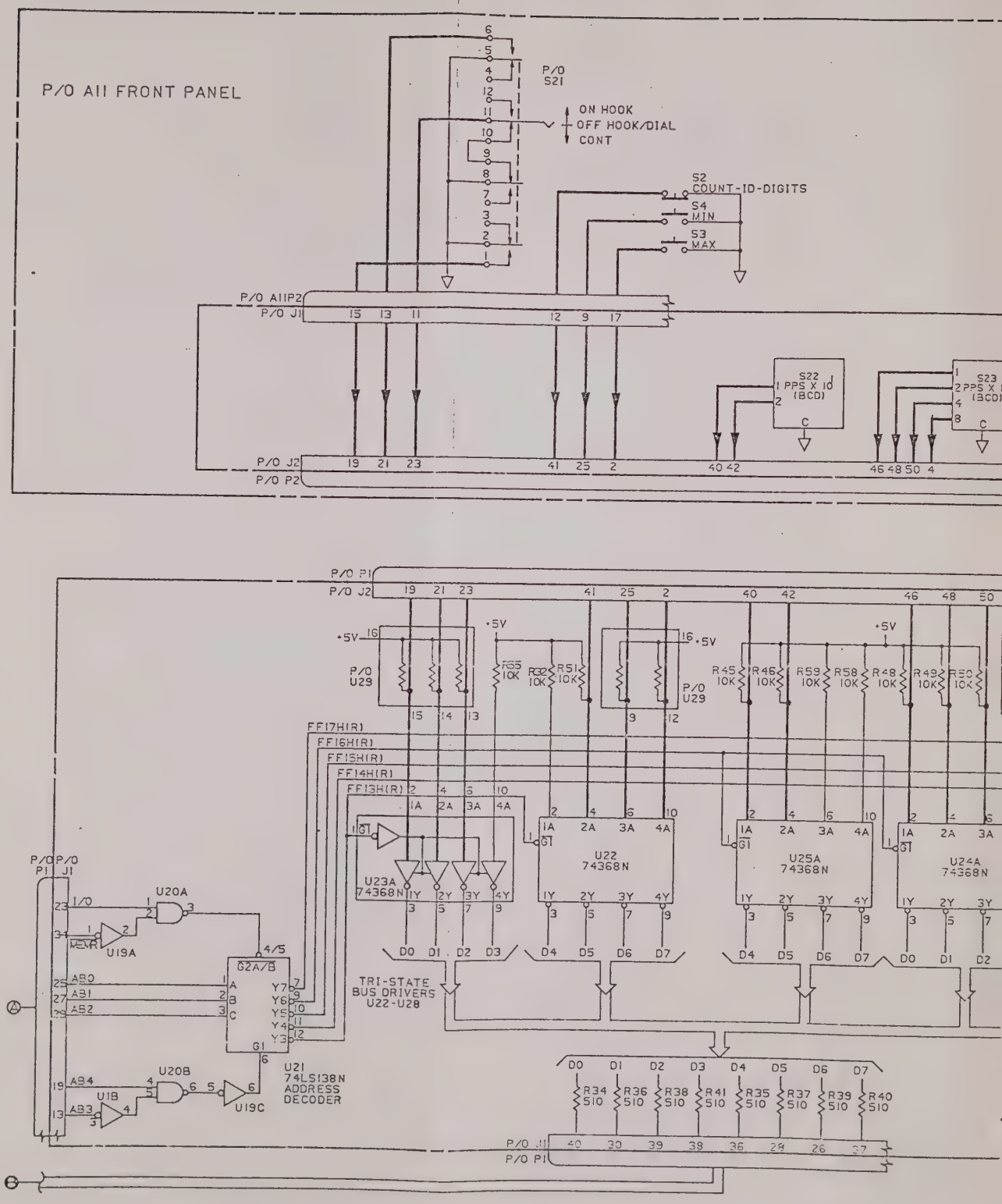


Figure 6—5. Switch Status Functional Schematic Diagram. (Sheet 2 of 2)

ADDRESS DECODING TRUTH TABLE

I/O	MEMR	AB0	AB1	AB2	AB3	AB4	FFXXH(R)
H	L	H	H	L	L	H	FF13H(R)
H	L	L	L	H	L	H	FF14H(R)
H	L	H	L	H	L	H	FF15H(R)
H	L	L	H	H	L	H	FF16H(R)
H	L	H	H	H	L	H	FF17H(R)

FF13H(R) = READ ON HK/OFF HK/CONT AND MIN-MAX SWITCHES.
FF14H(R) = READ %BK X 10^1 + X 10^0 SWITCHES.
FF15H(R) = READ %BK X 10^{-1} + PPS X 10^{-1} SWITCHES.
FF16H(R) = READ PPS X 10^1 + X 10^0 SWITCHES.
FF17H(R) = READ ID X 10^2 + X 10^1 SWITCHES.

A5
THUMBWHEEL BOARD

S24 2 PPS X 10^{-1} (BCD)
S25 2%BRK X 10^1 (BCD)
S26 2%BRK X 10^0 (BCD)
S27 2%BRK X 10^{-1} (BCD)
S28 2 ID X 10^2 (BCD)
S29 2 ID X 10^1 (BCD)

12 14 6 8 | 34 36 38 16 | 28 30 32 22 | 24 26 18 20 | 3 5 7 9 | 11 13 15 17

PIN-FOR-PIN CONNECTION
36

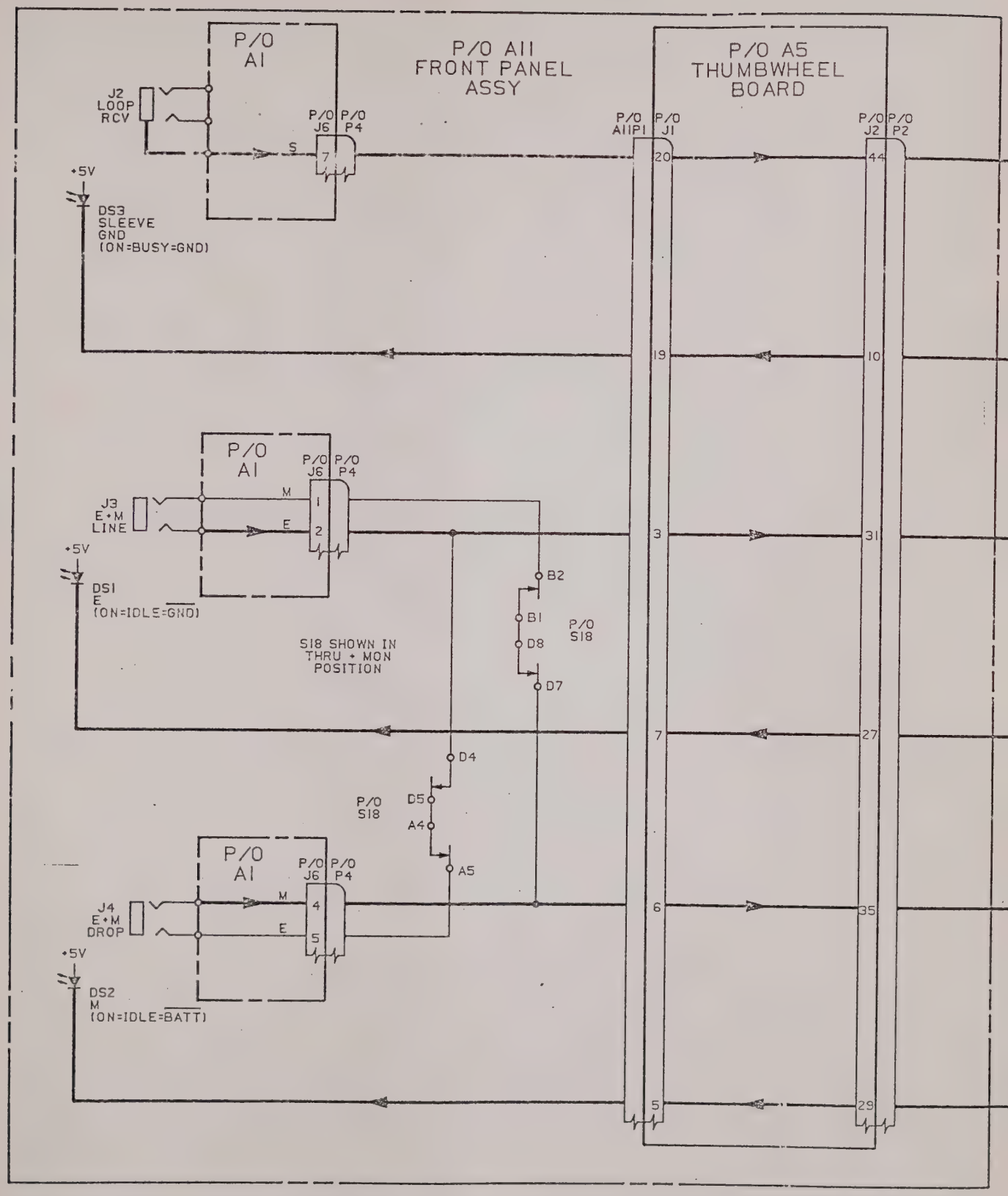
+5V
P/O U29
P/O U30
P/O U29

U25B 74368N
U24B 74368N
U26A 74368N
U27A 74368N
U27B 74368N
U26B 74368N
U28A 74368N
U28B 74368N
U23B 74368N

D4 D5 D6 D7 D4 D5 D6 D7 D0 D1 D2 D3 D0 D1 D2 D3 D0 D1 D2 D3 D4 D5 D6 D7

P/O A6 ANALOG RCVR BOARD

E-02466-01


P/O A1
P/O A11 FRONT PANEL ASSY
P/O A5 THUMBWHEEL BOARD
J2 LOOP RCV
P/O J6
P/O P4
P/O A11P1
P/O J1
P/O J2
P/O P2
S
7
20
44
+5V
DS3 SLEEVE GND (ON=BUSY=GND)
19
10
J3 E•M LINE
M
E
1
2
3
31
DS1 E (ON=IDLE=GND)
B2
B1
D8
D7
P/O S18
S18 SHOWN IN THRU • MON POSITION
7
27
D4
D5
A4
A5
6
35
J4 E•M DROP
4
5
DS2 M (ON=IDLE=BATT)
5
29

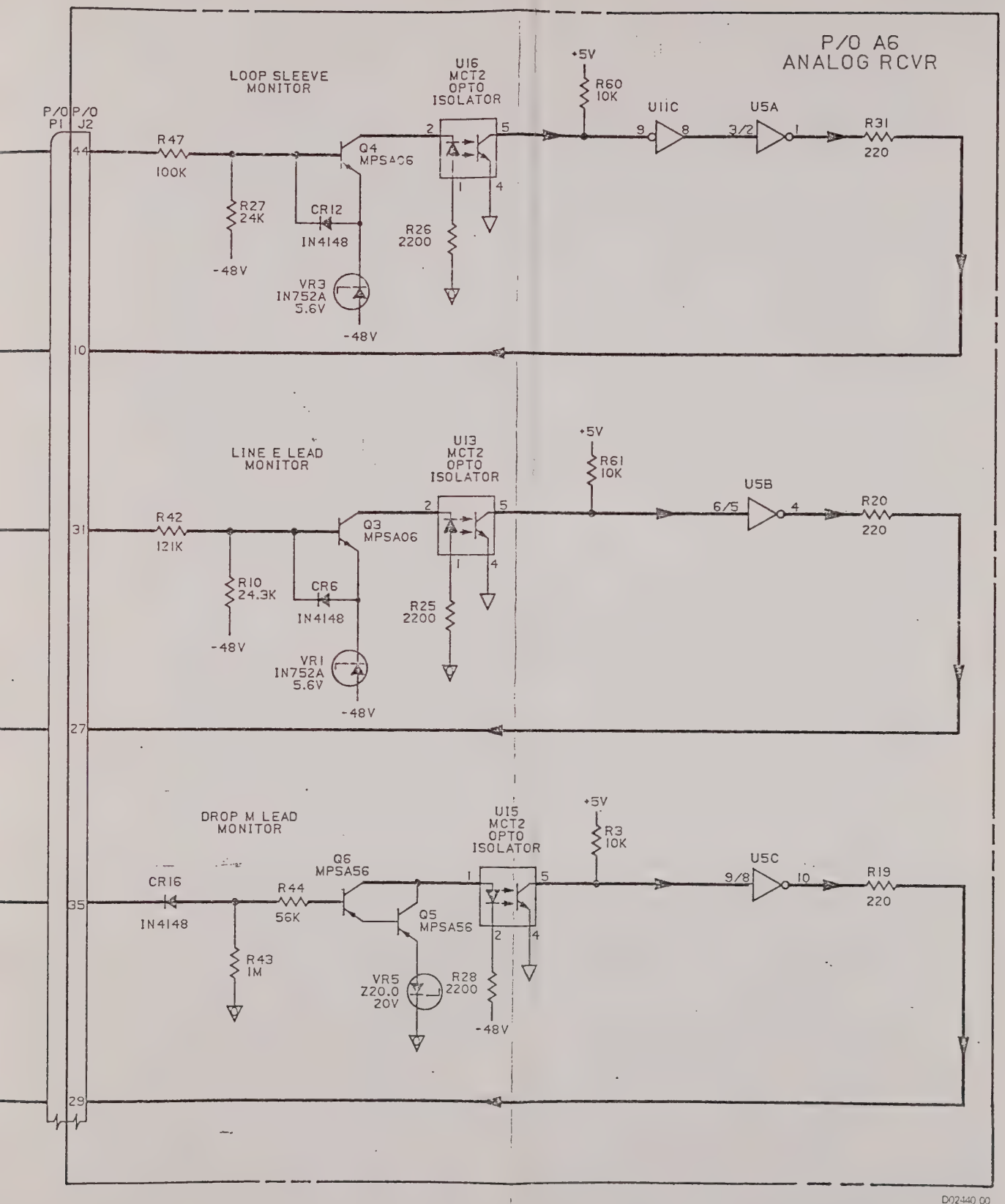


Figure 6—6. Monitor Functional Schematic Diagram.

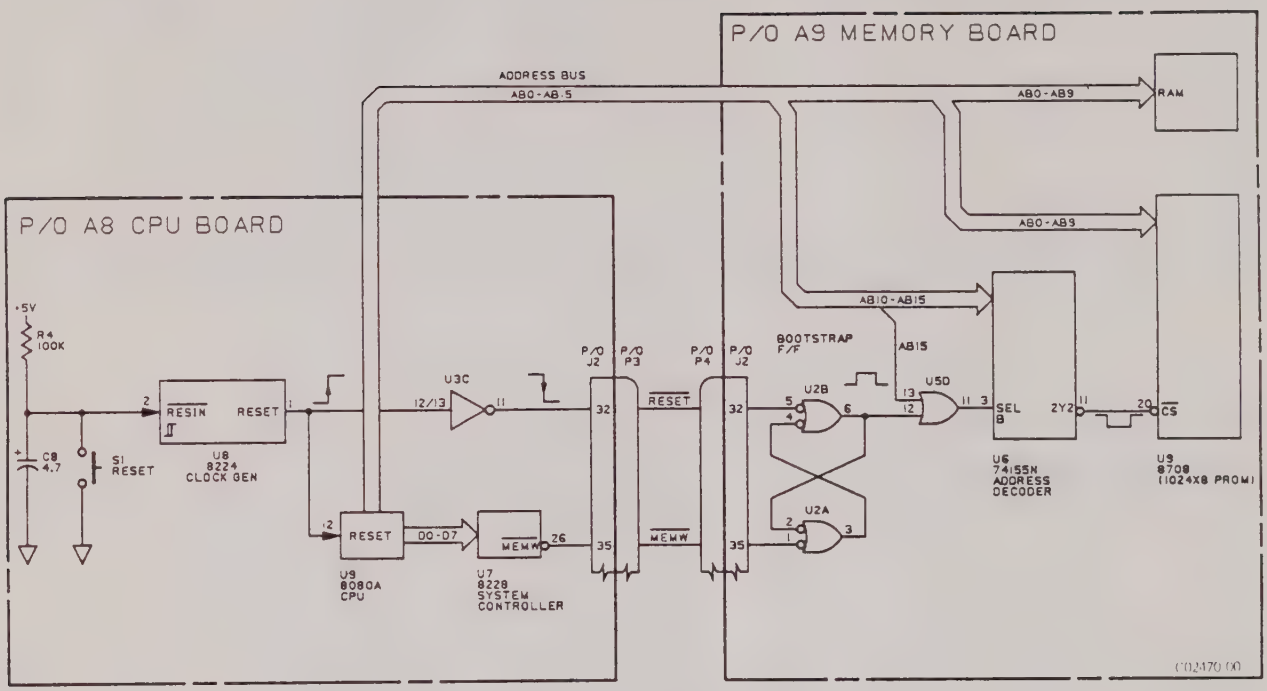
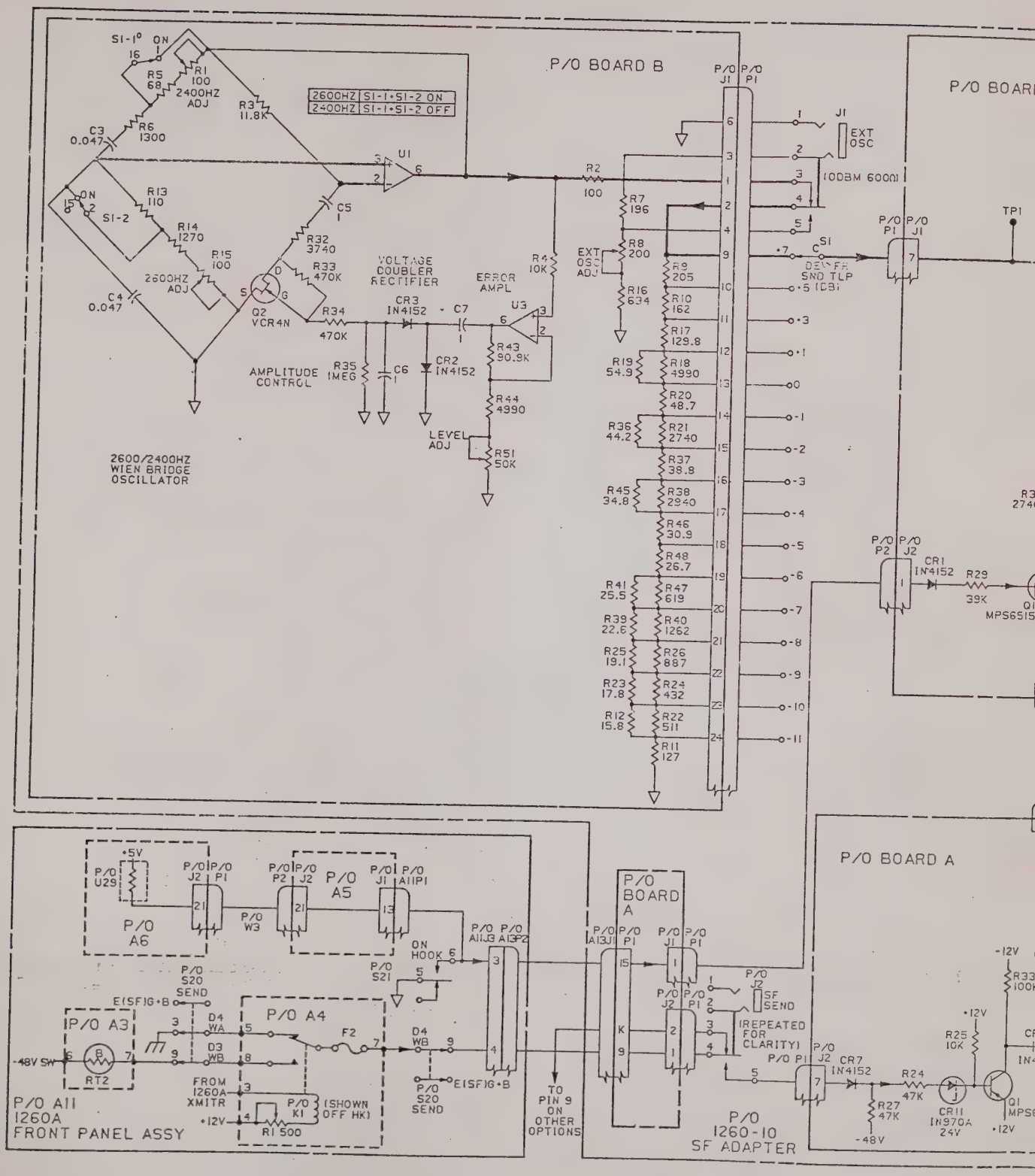


Figure 6—7. Reset Functional Schematic Diagram.


P/O BOARD B
2600HZ | S1-1•S1-2 ON
2400HZ | S1-1•S1-2 OFF
S1-1 ON
R5 68
R1 100 2400HZ ADJ
R3 11.8K
C3 0.047
R6 1300
U1
R2 100
R13 110
S1-2
R14 1270
R15 100
2600HZ ADJ
C4 0.047
C5 1
R32 3740
R33 470K
Q2 VCR4N
VOLTAGE DOUBLER RECTIFIER
ERROR AMPL
R4 10K
R34 470K
CR3 IN4152
C7 1
U3
R43 90.9K
AMPLITUDE CONTROL
R35 1MEG
C6 1
CR2 IN4152
R44 4990
LEVEL ADJ
R51 50K
2600/2400HZ WIEN BRIDGE OSCILLATOR
P/O J1 P/O P1
J1
EXT OSC
(10DBM 600Ω)
EXT OSC ADJ
R8 200
R7 196
R9 205
R16 634
R10 162
R17 129.8
R19 54.9
R18 4990
R20 48.7
R36 44.2
R21 2740
R37 38.8
R45 34.8
R38 2940
R46 30.9
R48 26.7
R41 25.5
R47 619
R39 22.6
R40 1262
R25 19.1
R26 887
R23 17.8
R24 432
R12 15.8
R22 511
R11 127
+7
+5 (DB)
+3
+1
0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
S1
DEN FR SND TLP
P/O P1 P/O J1
TP1
P/O BOARD A
P/O P2 P/O J2
CR1 IN4152
R29 39K
Q1 MPS6515
P/O A6
+5V
P/O U29
P/O J2 P/O P1
P/O W3
P/O A5
P/O P2 P/O J2
P/O J1 P/O A11P1
P/O A11J3 P/O A13P2
ON HOOK
P/O S21
P/O S20 SEND
E(SF)G•B
P/O A3
-48V SW
RT2
D4 WA
D3 WB
P/O A4
F2
D4 WB
FROM 1260A XMITR
+12V
P/O K1 (SHOWN OFF HK)
R1 500
P/O A11 1260A FRONT PANEL ASSY
TO PIN 9 ON OTHER OPTIONS
P/O BOARD A
P/O A13J1 P/O P1
P/O J1 P/O P1
P/O J2 P/O P1
P/O J2 SF SEND
(REPEATED FOR CLARITY)
P/O 1260-10 SF ADAPTER
P/O P1 P/O J2
CR7 IN4152
R24 47K
R27 47K
-48V
CR11 IN970A 24V
+12V
R25 10K
-12V
R33 100K
Q1 MPS6

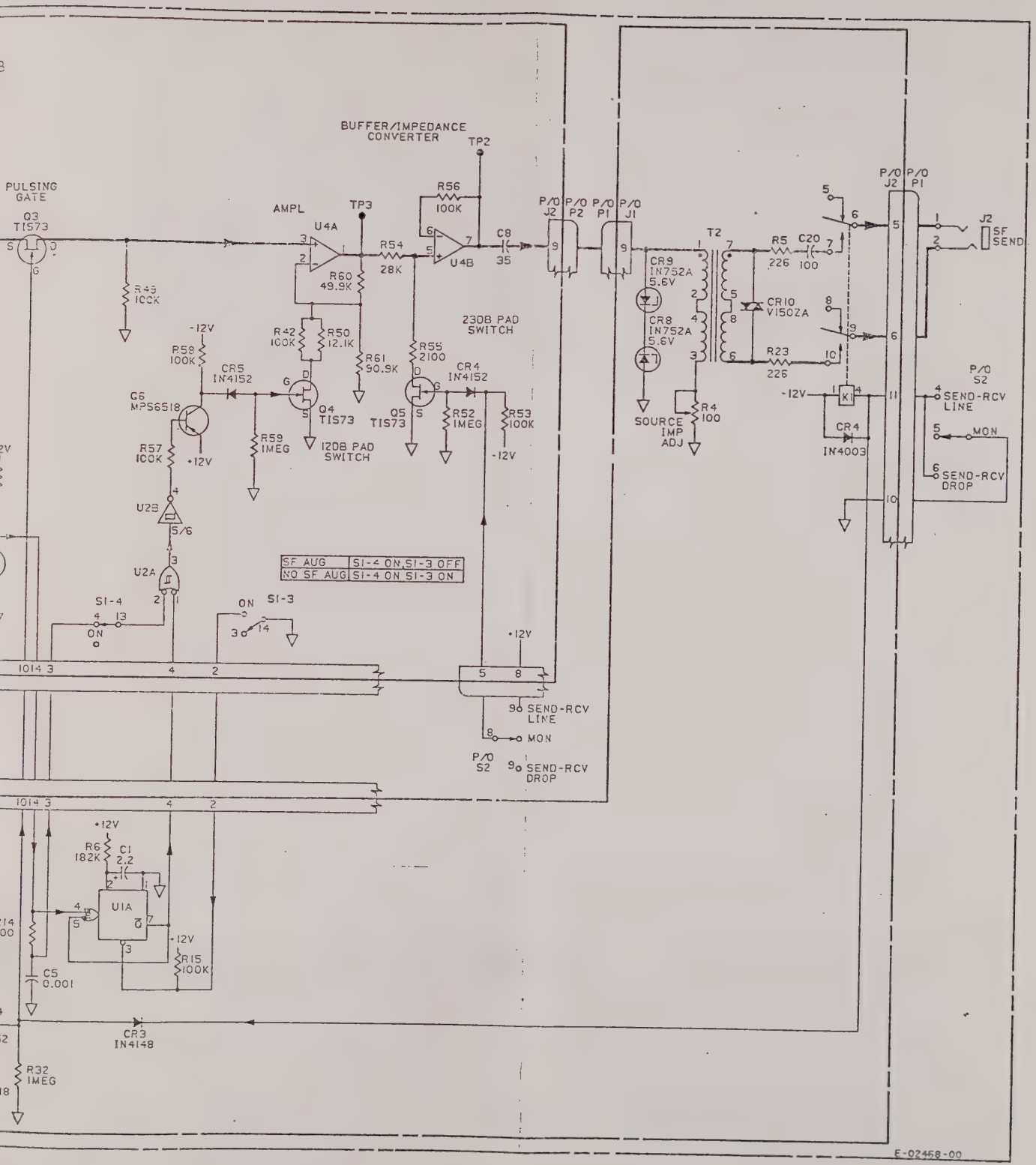
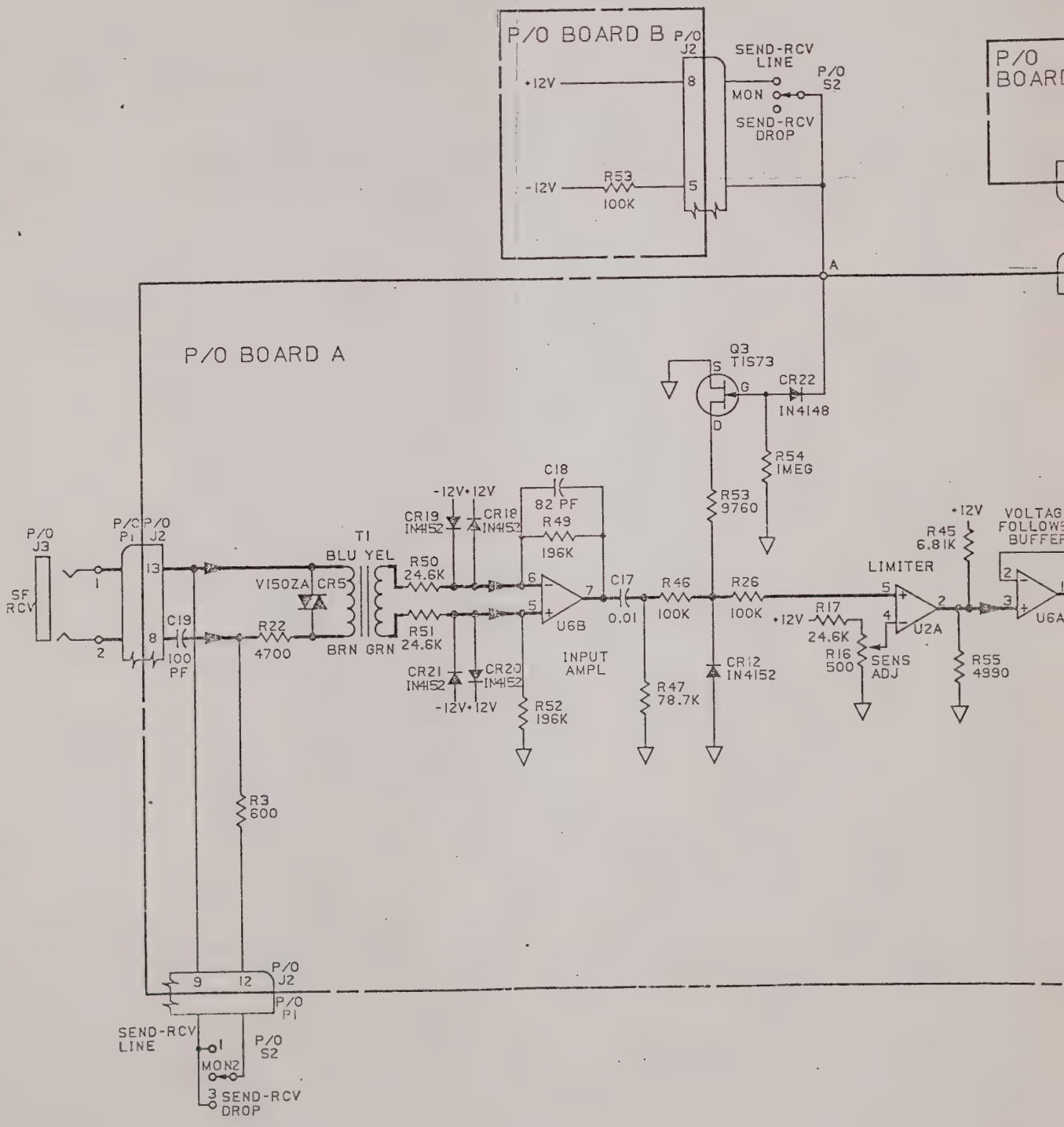


Figure 6—8. SF Adapter Send Functional Schematic Diagram.


P/O BOARD B
P/O J2
SEND-RCV LINE
+12V
8
MON
P/O S2
SEND-RCV DROP
-12V
R53 100K
5
P/O BOARD A
A
Q3 TIS73
S
G
D
CR22 IN4148
R54 IMEG
R53 9760
C18 82 PF
-12V +12V
CR19 IN4152
CR18 IN4152
R49 196K
P/O J3
P/O P1
P/O J2
SF RCV
1
2
13
8
C19 100 PF
R22 4700
V150ZA CR5
TI
BLU YEL
BRN GRN
R50 24.6K
R51 24.6K
6
5
7
U6B
C17 0.01
R46 100K
R26 100K
INPUT AMPL
CR21 IN4152
CR20 IN4152
-12V +12V
R52 196K
R47 78.7K
CR12 IN4152
+12V
R45 6.81K
LIMITER
5
4
2
U2A
R17 24.6K
R16 500
SENS ADJ
R55 4990
VOLTAG FOLLOWS BUFFER
U6A
R3 600
9
12
P/O J2
P/O P1
SEND-RCV LINE
1
P/O S2
MON 2
3 SEND-RCV DROP

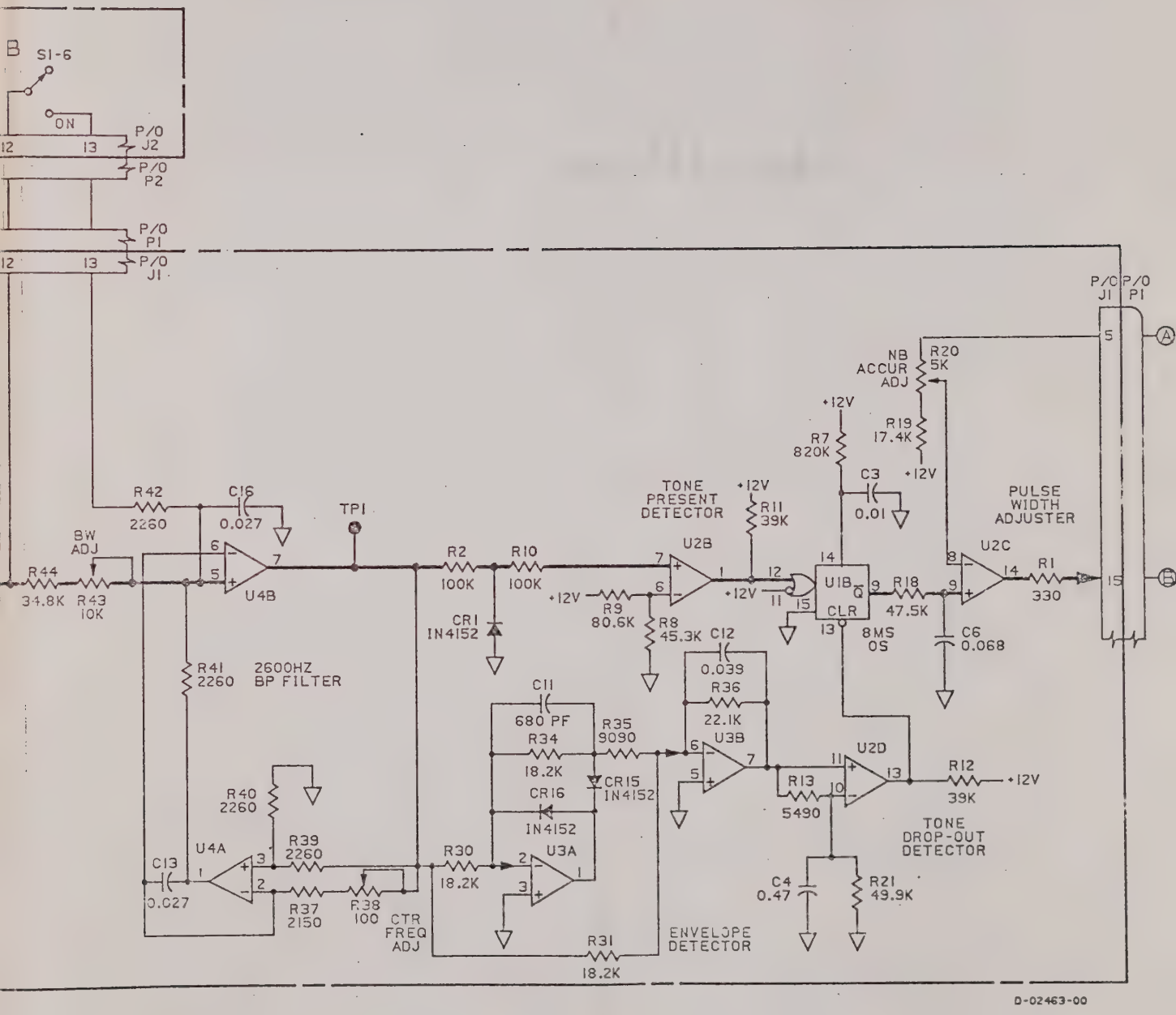
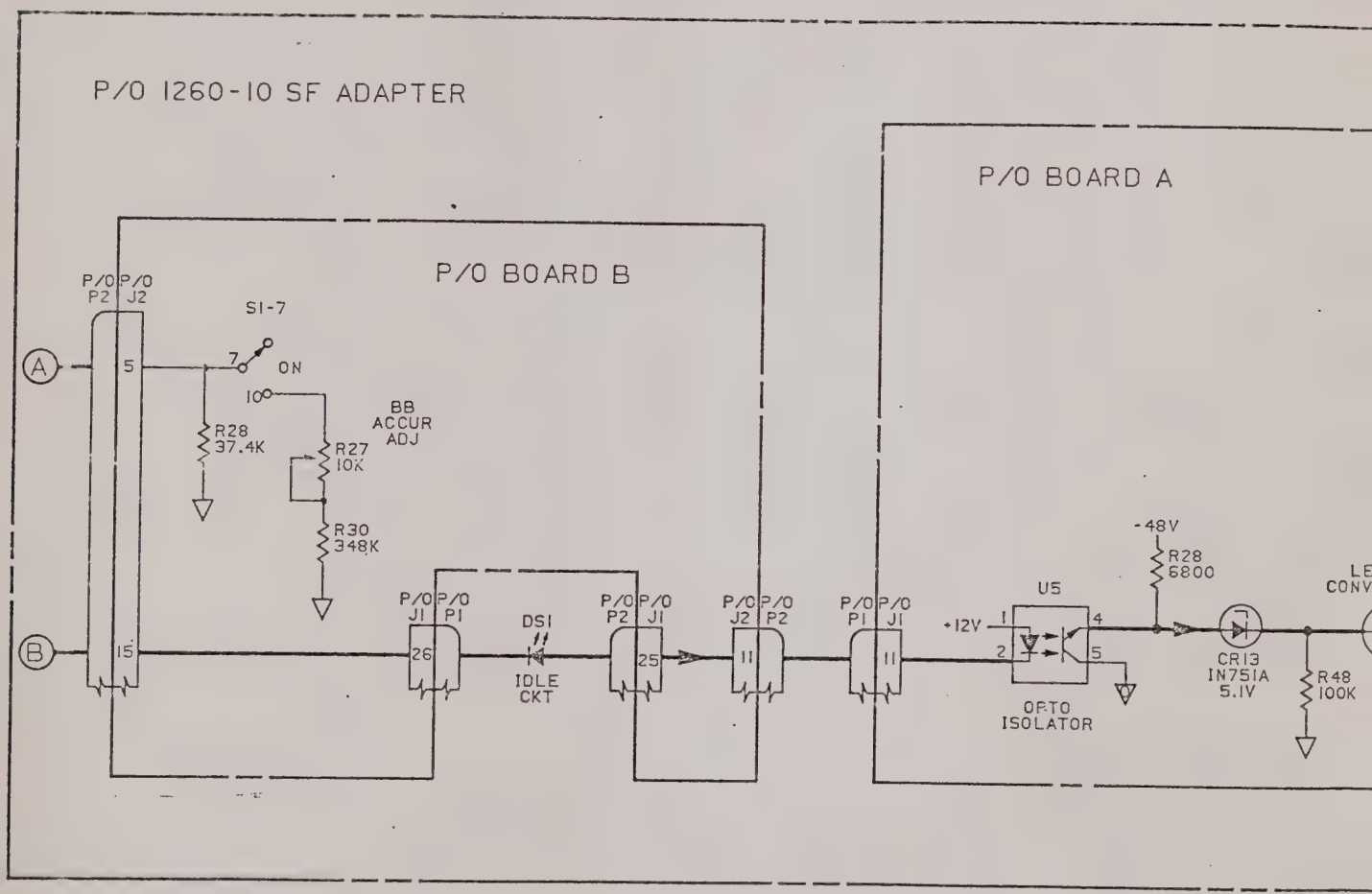


Figure 6—9. SF Adapter Receive Functional Schematic Diagram. (Sheet 1 of 2)


P/O 1260-10 SF ADAPTER
P/O BOARD A
P/O BOARD B
P/O P2
P/O J2
S1-7
7
ON
10
BB ACCUR ADJ
R28 37.4K
R27 10K
R30 348K
A
B
5
15
P/O J1
P/O P1
26
DS1
IDLE CKT
P/O P2
P/O J1
25
P/O J2
P/O P2
11
P/O P1
P/O J1
11
U5
+12V
1
2
4
5
OPTO ISOLATOR
-48V
R28 6800
CR13 IN751A 5.1V
R48 100K

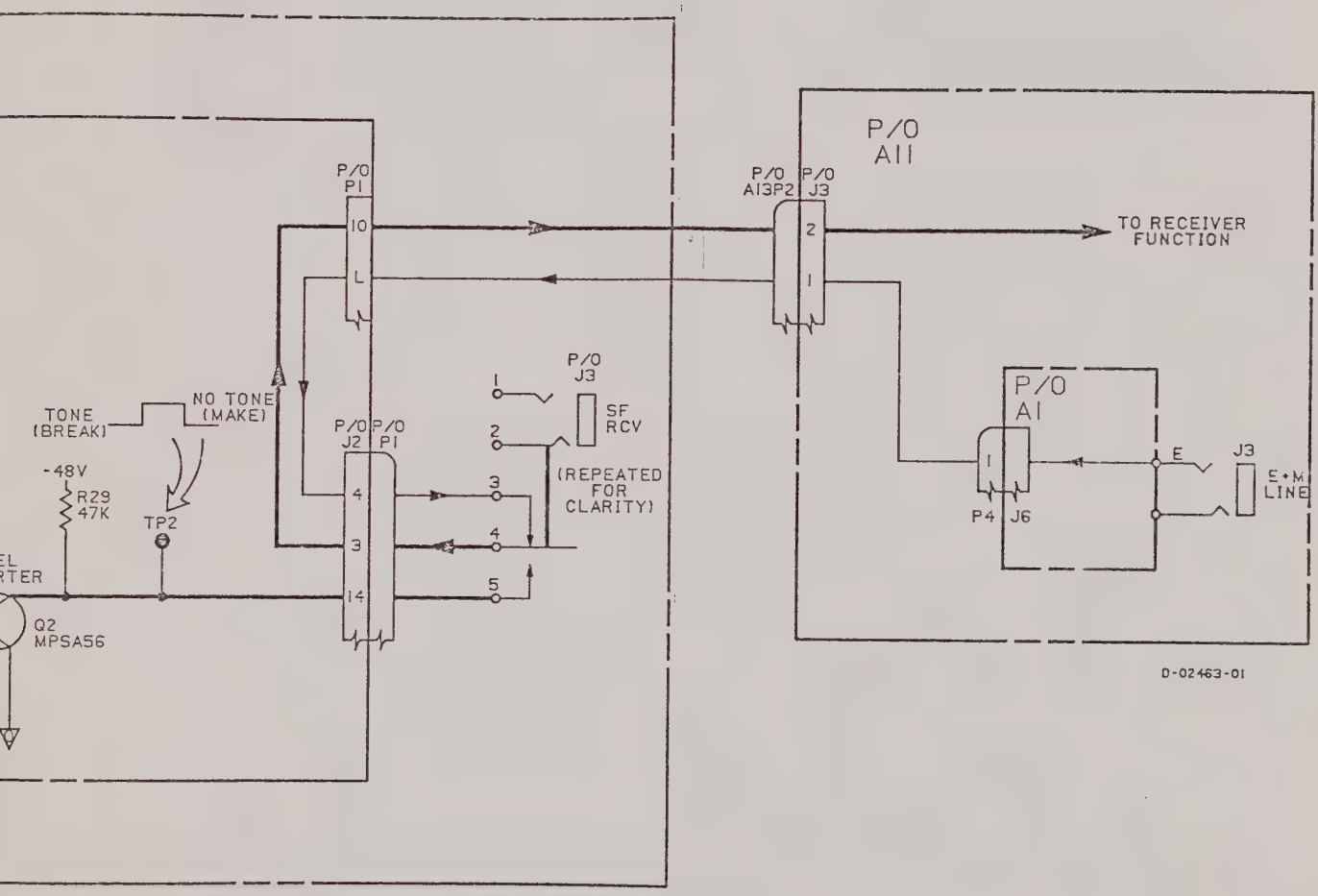
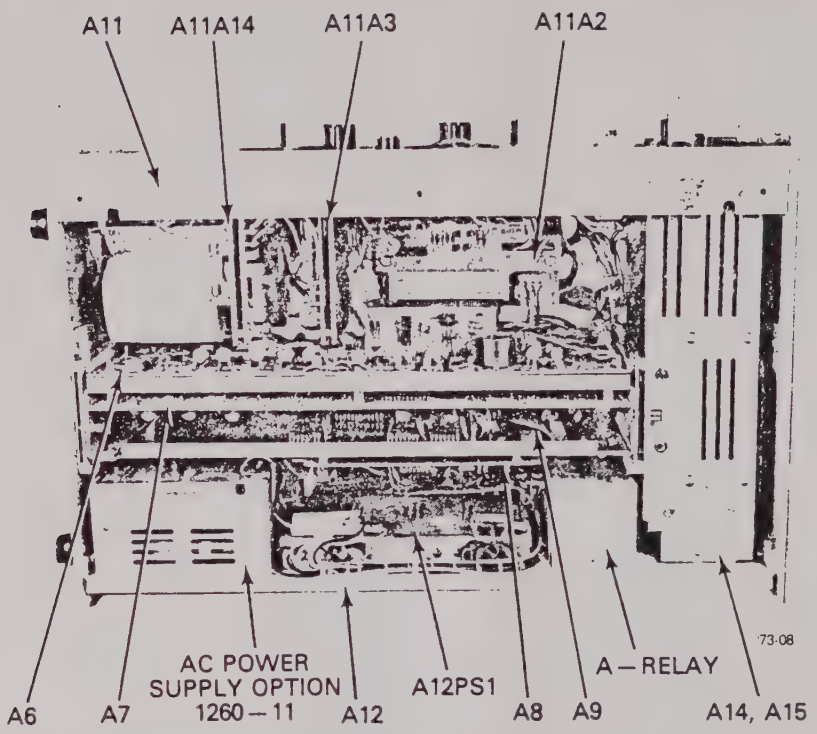
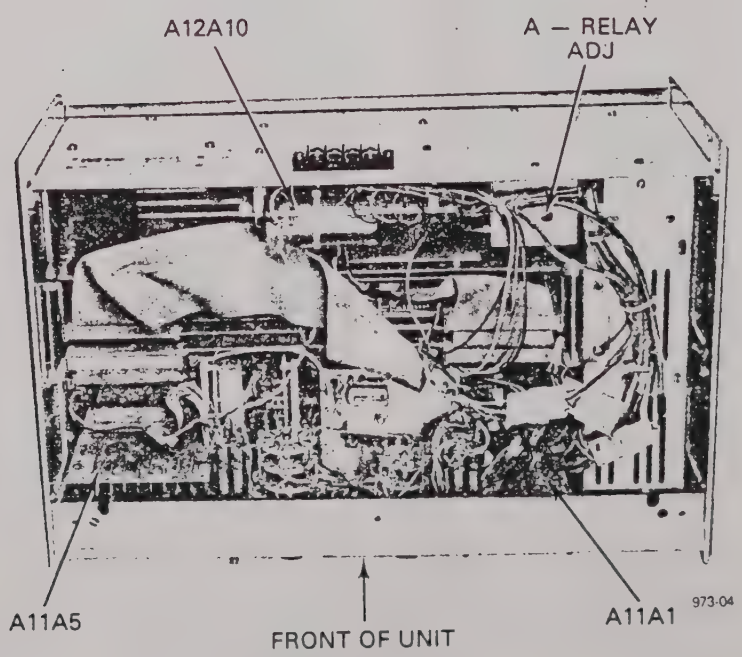


Figure 6—9. SF Adapter Receive Functional Schematic Diagram. (Sheet 2 of 2)

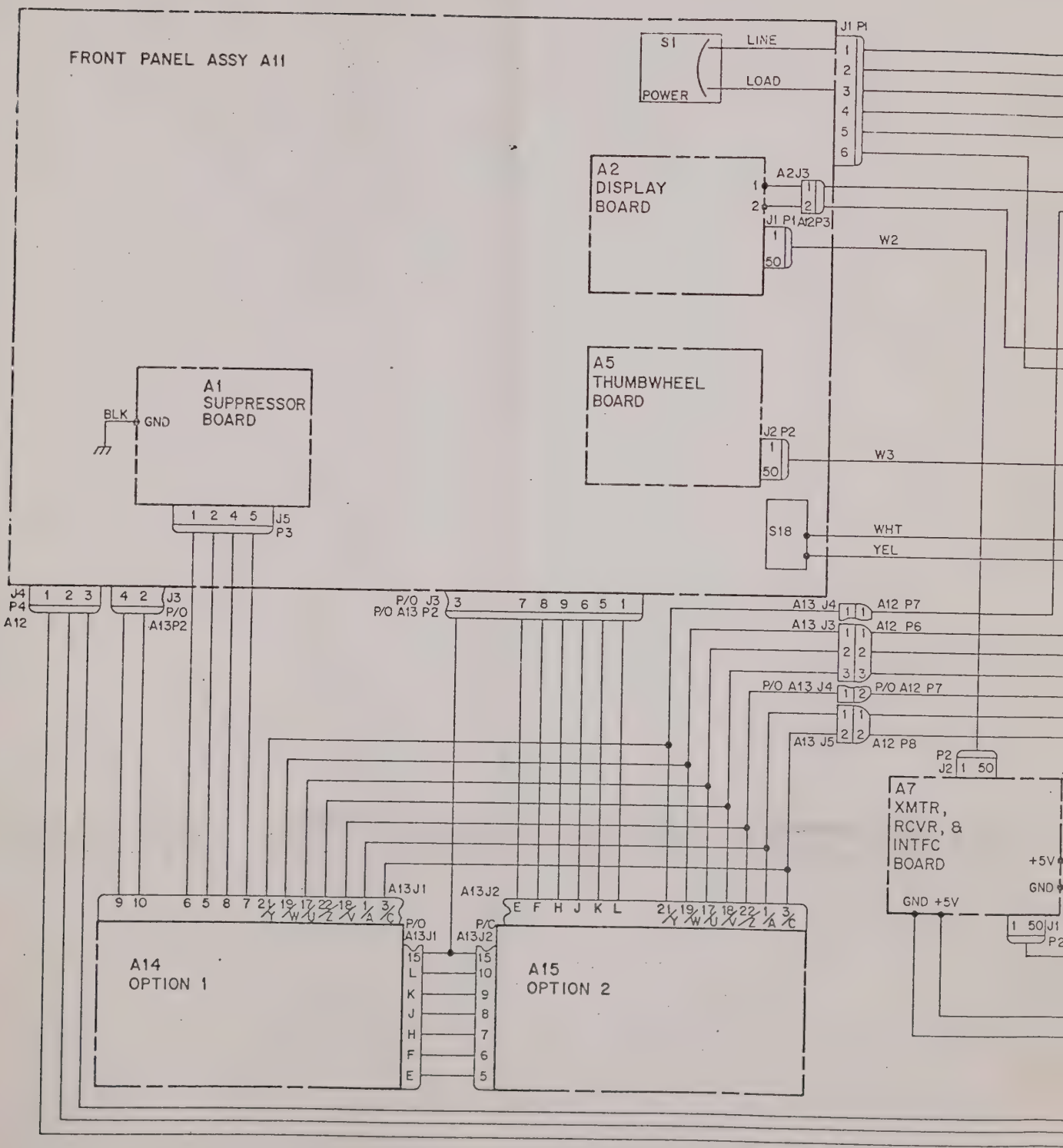


TOP VIEW



BOTTOM VIEW

Figure 6—10. Location of 1260A Subassemblies.


FRONT PANEL ASSY A11
S1
POWER
LINE
LOAD
J1 P1
1
2
3
4
5
6
A2
DISPLAY
BOARD
A2J3
1
2
J1 P1 A2P3
1
50
W2
A5
THUMBWHEEL
BOARD
J2 P2
1
50
W3
A1
SUPPRESSOR
BOARD
BLK
GND
1 2 4 5
J5
P3
S18
WHT
YEL
J4
P4
A12
1 2 3
4 2
J3
P/O
A13P2
P/O J3
P/O A13 P2
3 7 8 9 6 5 1
A13 J4
A12 P7
A13 J3
A12 P6
P/O A13 J4
P/O A12 P7
A13 J5
A12 P8
P2
J2
1 50
A7
XMTR,
RCVR, &
INTFC
BOARD
+5V
GND
GND +5V
1 50 J1
P2
A13J1
A13J2
9 10 6 5 8 7 21 19 17 22 18 1 3
E F H J K L 21 19 17 18 22 1 3
P/O
A13J1
P/C
A13J2
15
L
K
J
H
F
E
10
9
8
7
6
5
A14
OPTION 1
A15
OPTION 2

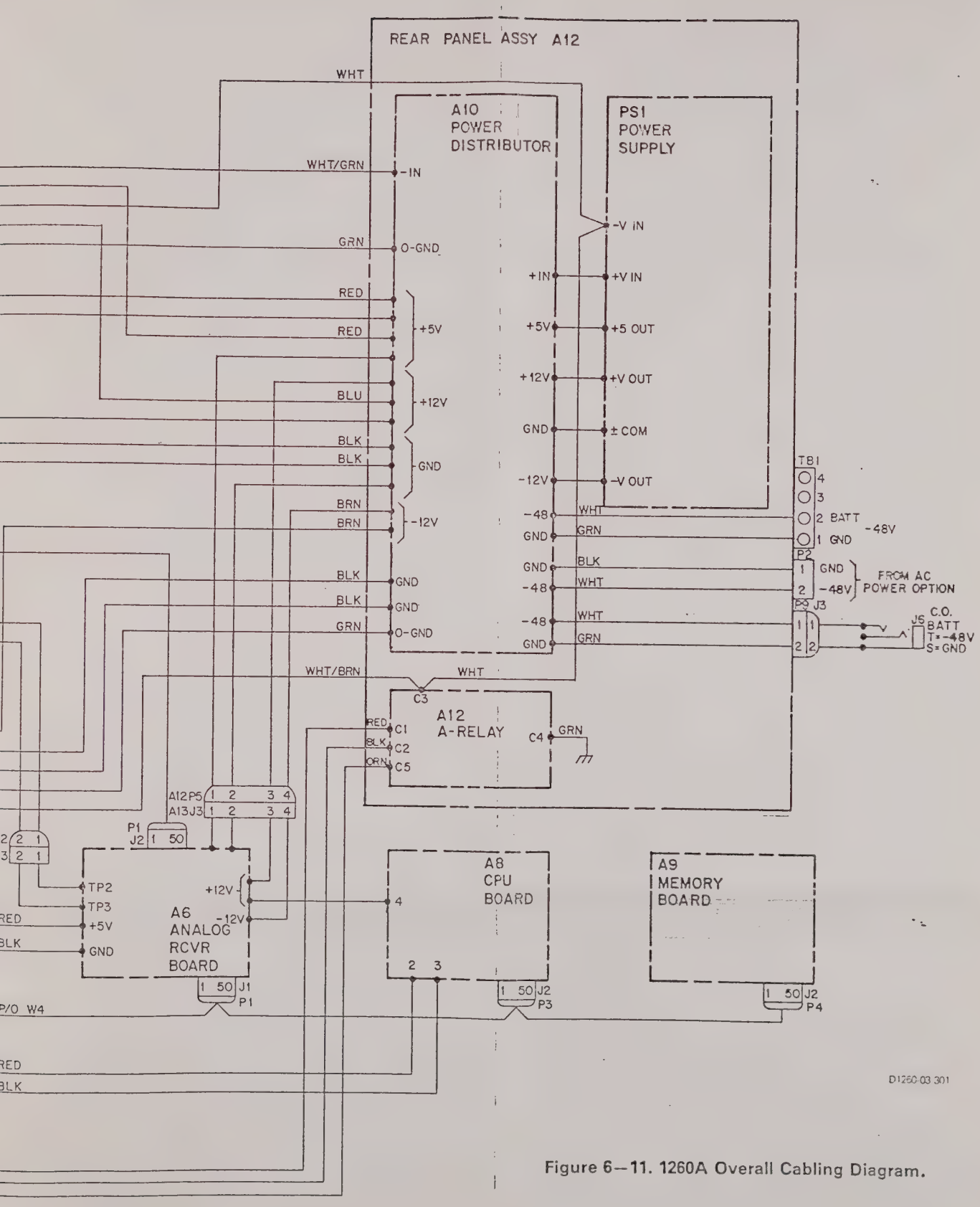


Figure 6—11. 1260A Overall Cabling Diagram.

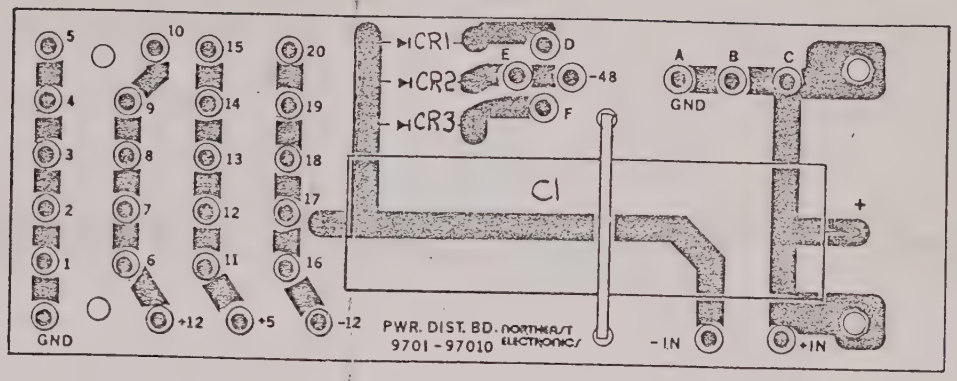


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Figure 6—12. 1260A Power Distribution Assembly A12A10, Component Location Diagram.

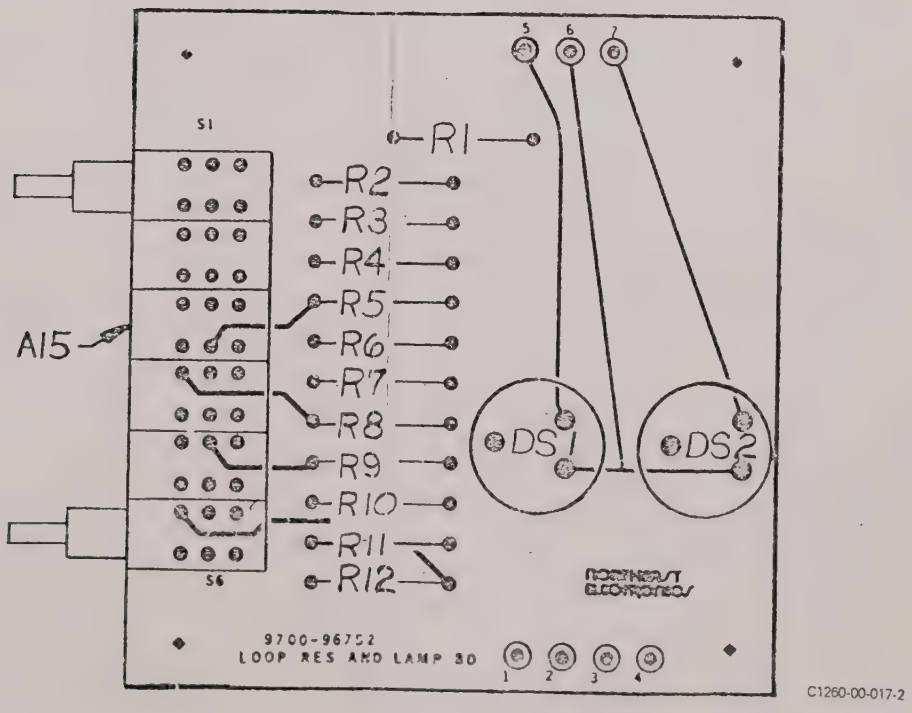

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Figure 6—14. Loop Resistor Assembly A11A3, Component Location Diagram.

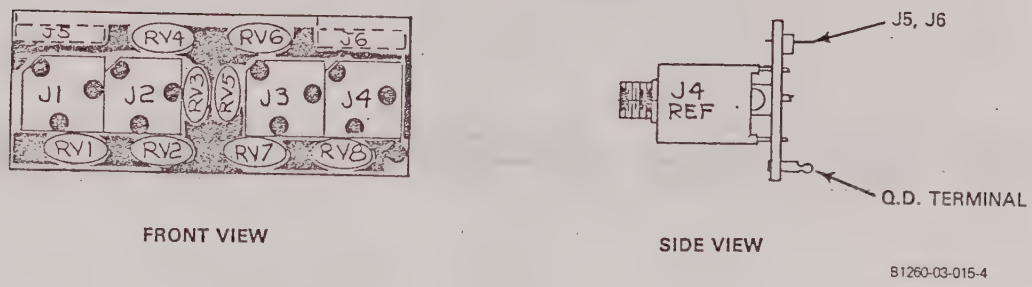


Figure 6—13. 1260A Suppressor Assembly A11A1, Component Location Diagram.

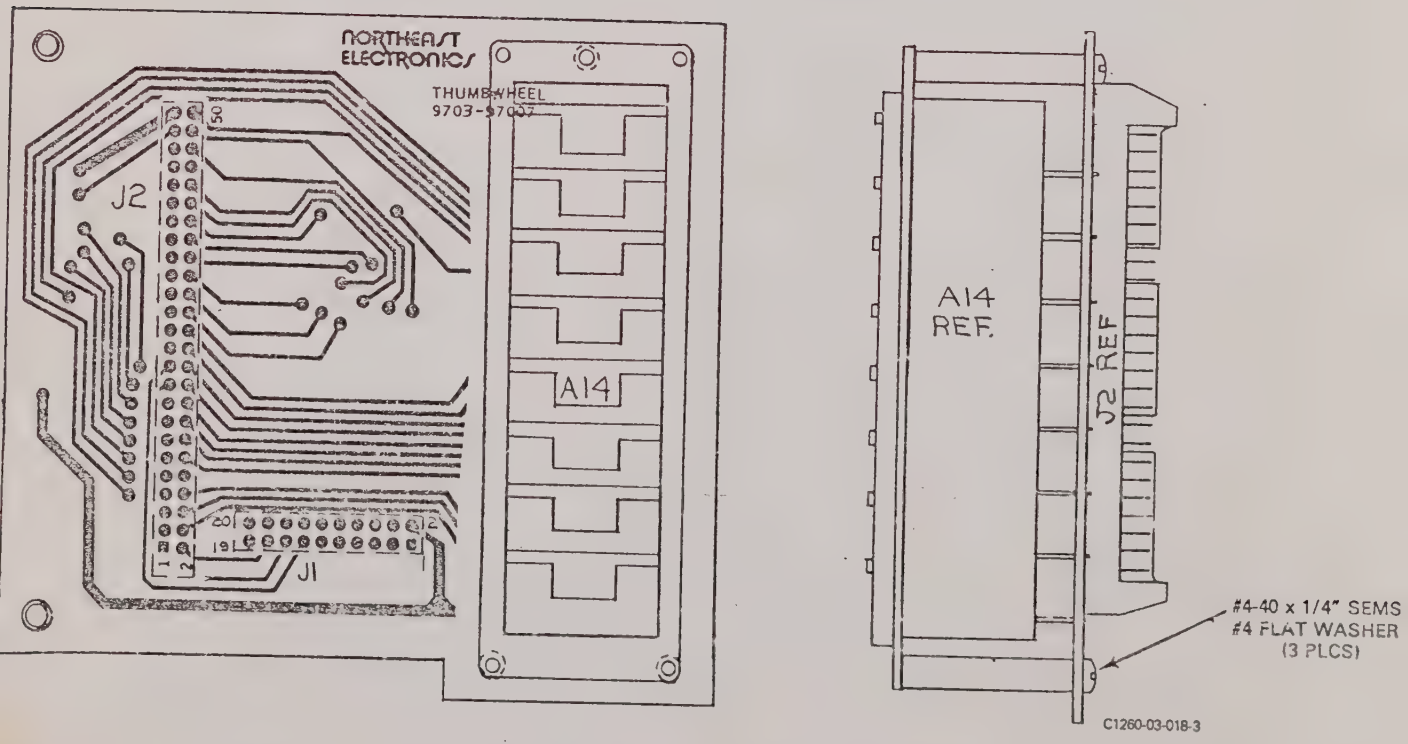
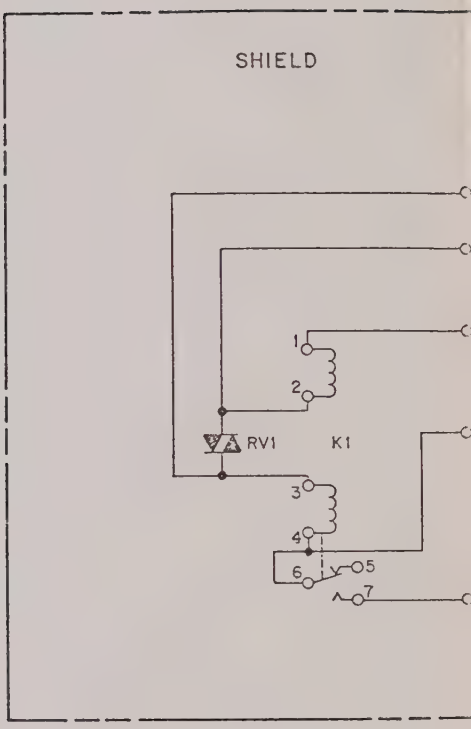


Figure 6—15. 1260A Percent Break, Pulse Speed, and Interdigit Time Switch Assembly A11A5, Component Location Diagram.


SHIELD
1
2
RV1
K1
3
4
6
5
7

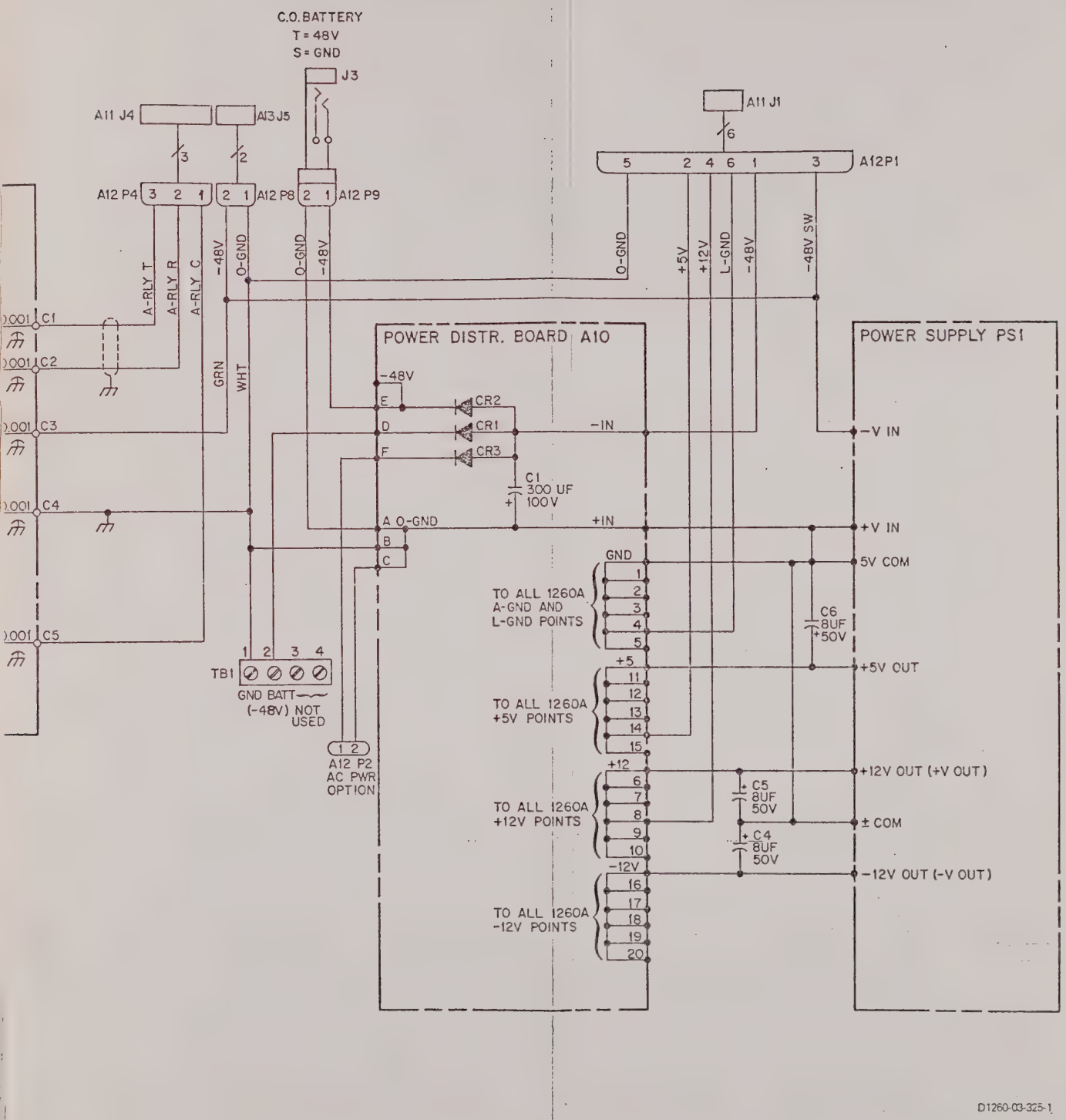
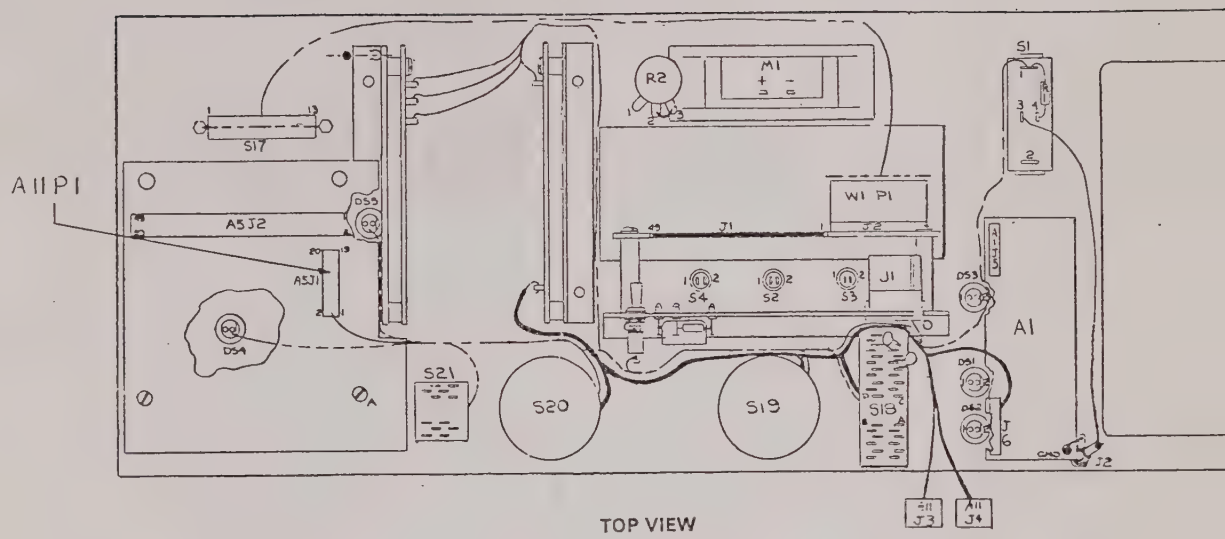
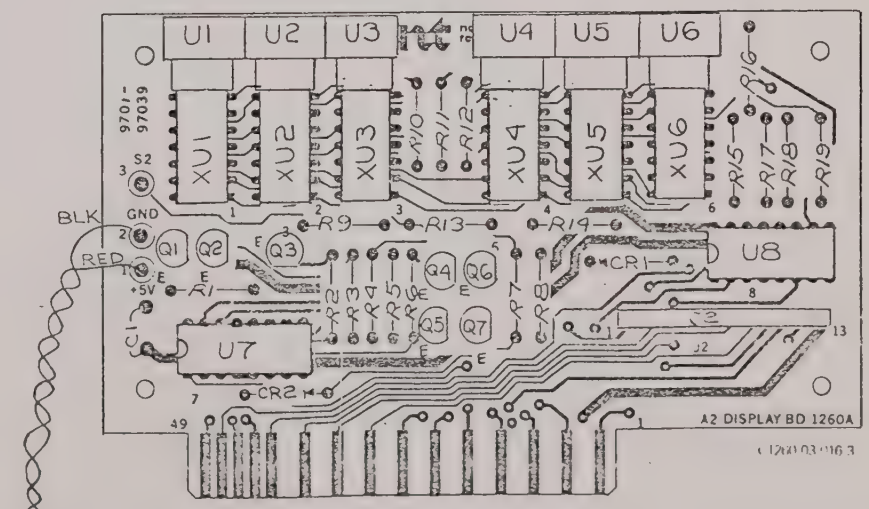


Figure 6—16. 1260A Rear Panel Assembly A12, Schematic Diagram.



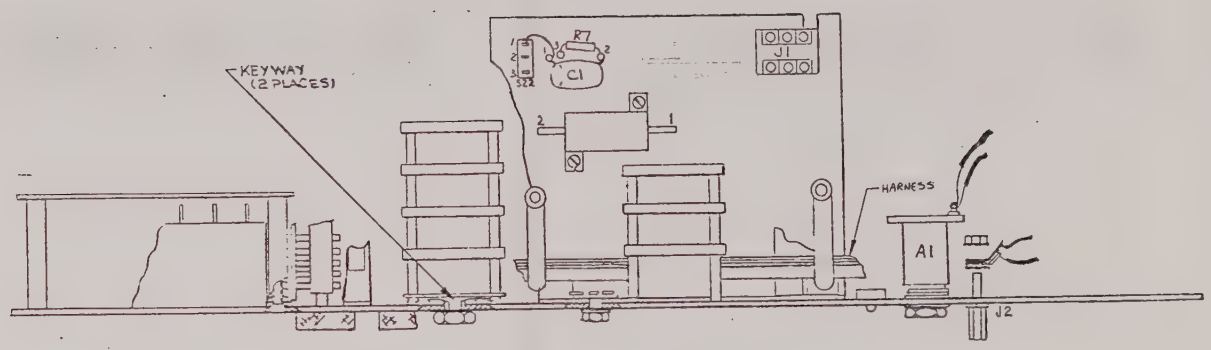
TOP VIEW

Figure 6—17. 1260A Front Panel Asse



A2 J3

Figure 6—18. 1260A Display Assembly A11A2, Component Location Diagram.



A11, Component Location Diagram.

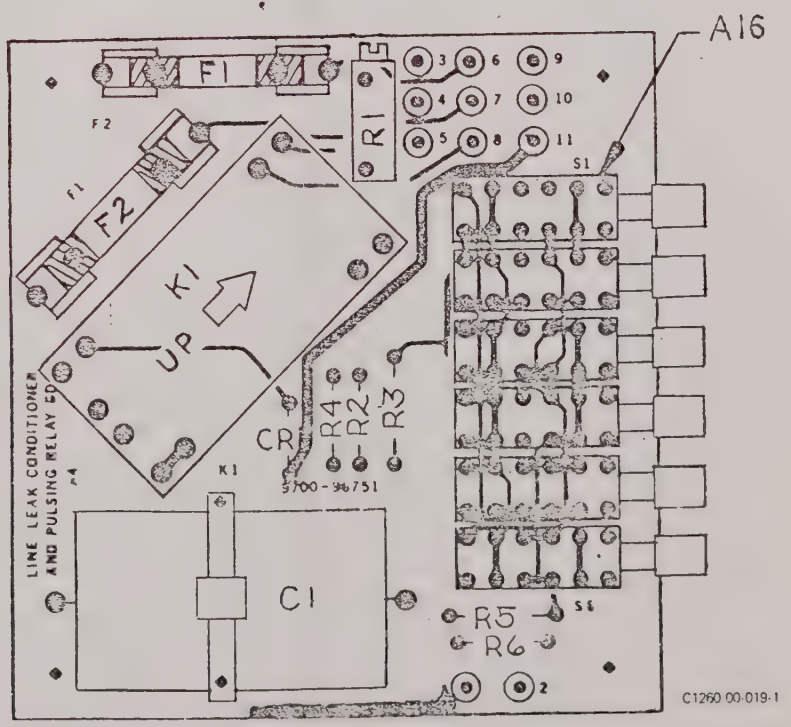
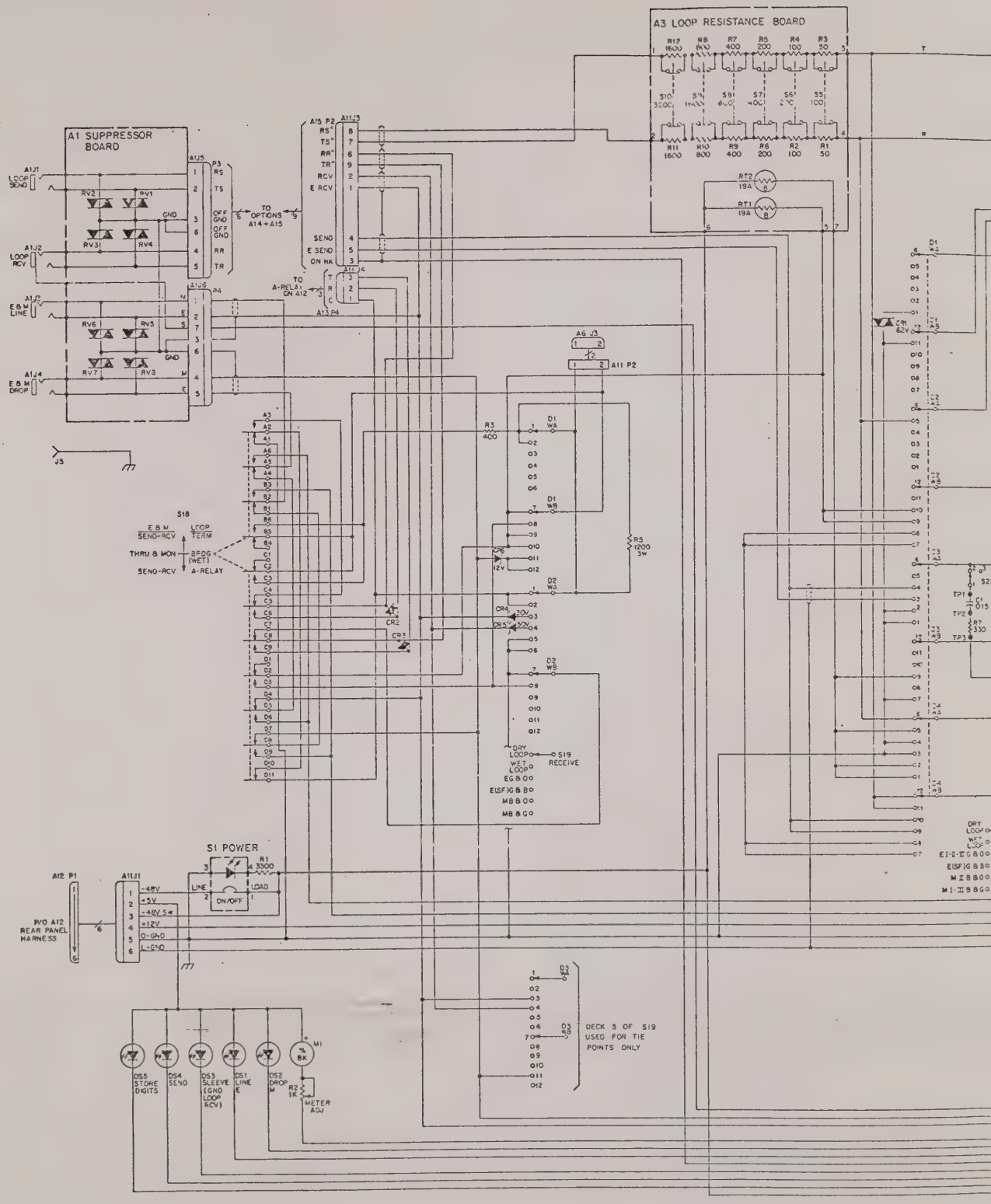


Figure 6—19. 1260A Leak Assembly A11A4, Component Location Diagram.


A3 LOOP RESISTANCE BOARD
A1 SUPPRESSOR BOARD
A1J1 LOOP SEND
A1J2 LOOP RCV
A1J3 E & M LINE
A1J4 E & M DROP
A1J5
A1J6
A11J3
A11J4
A13 P4
A15 P2
TO OPTIONS A14 + A15
TO A-RELAY ON A12
A6 J3
A11 P2
J3
S18
E & M SEND-RCV
LOOP TERM
THRU & MON
SEND-RCV
A-RELAY
S1 POWER
A12 P1
A11J1
P/O A12 REAR PANEL HARNESS
-48V
+5V
-48V S ⌀
+12V
O-GND
L-GND
LINE
LOAD
ON/OFF
DS5 STORE DIGITS
DS4 SEND
DS3 SLEEVE (GND LOOP RCV)
DS1 LINE E
DS2 DROP M
METER ADJ
DRY LOOP
WET LOOP
RECEIVE
DECK 3 OF S19 USED FOR TIE POINTS ONLY

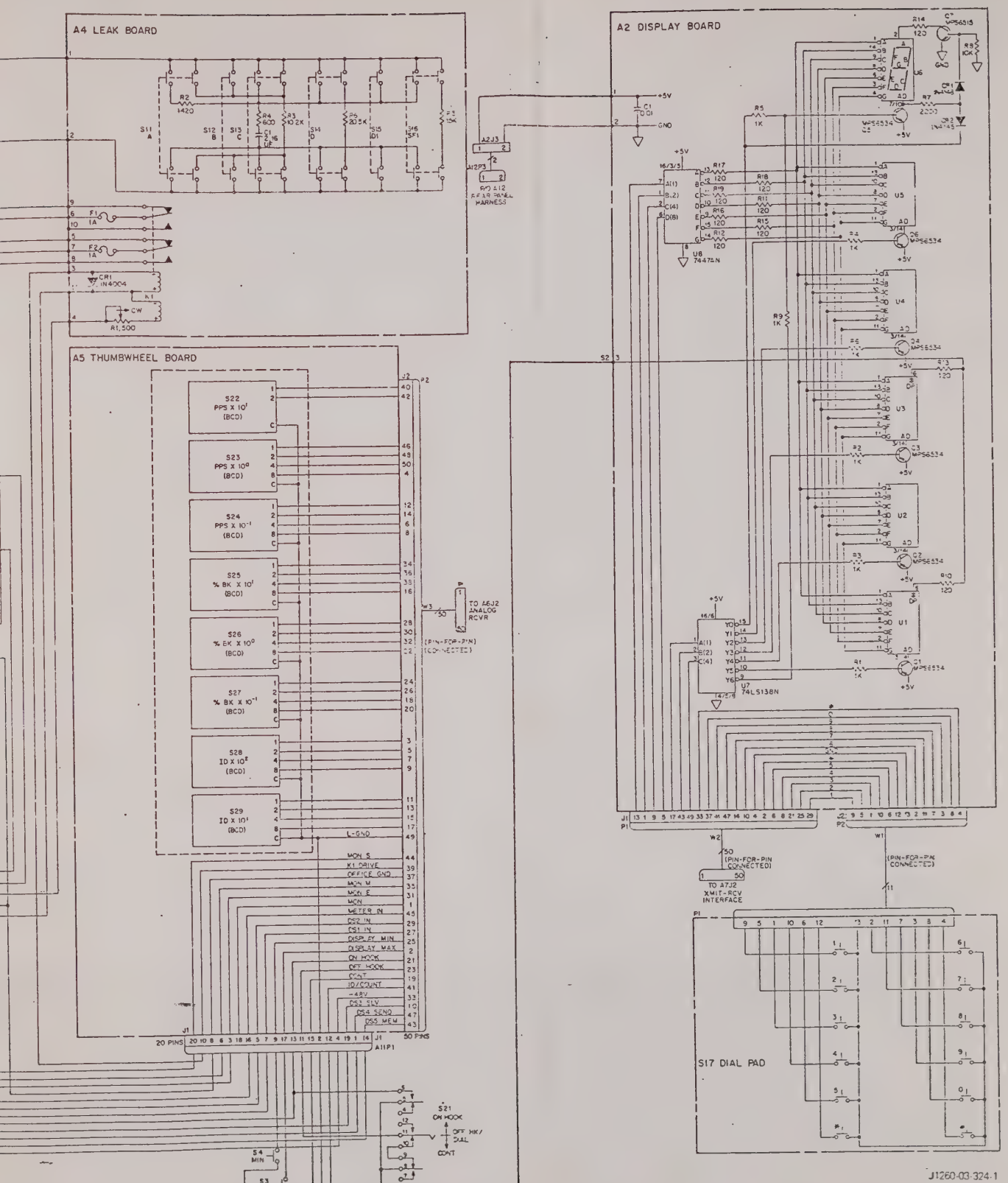


Figure 6—20. 1260A Front Panel Assembly A11, Schematic Diagram.

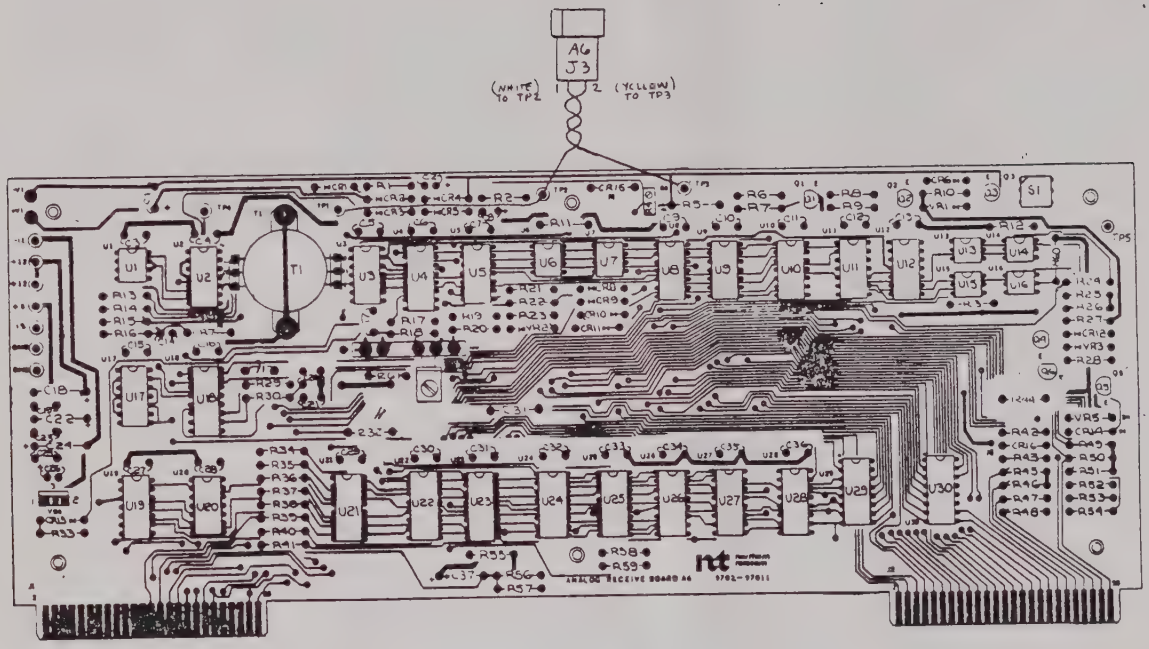
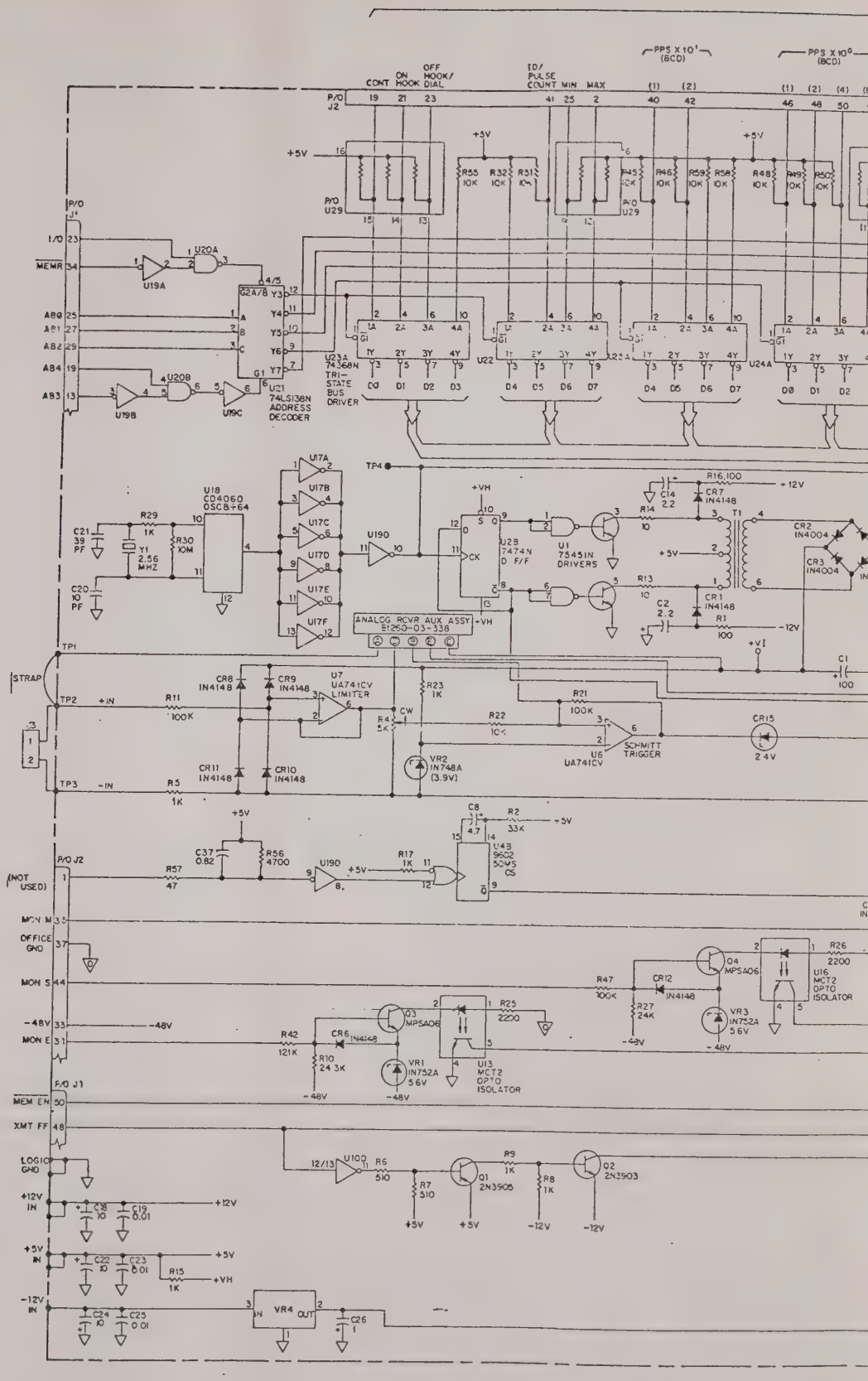
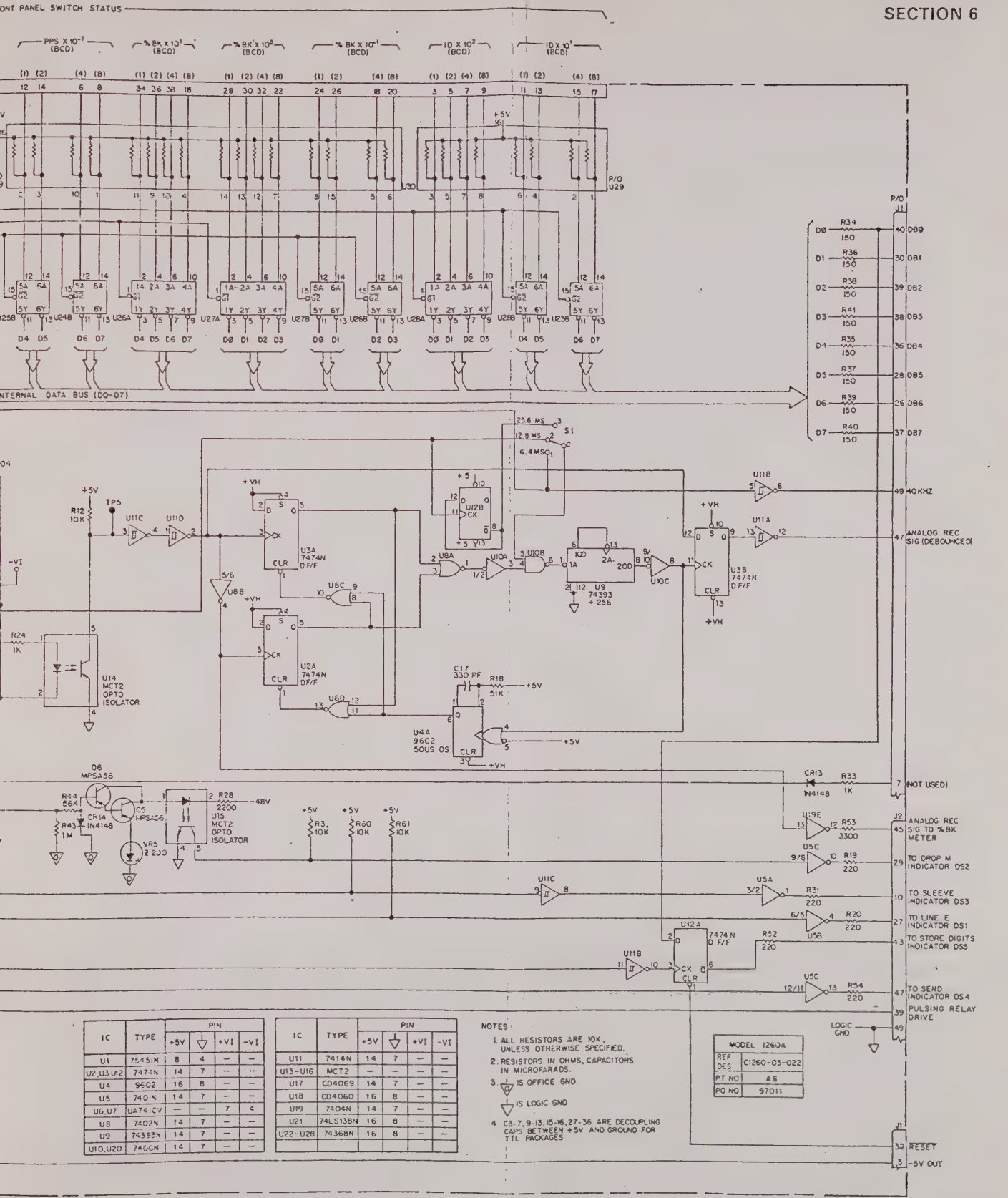


Figure 6—21. 1260A Analog Receiver Assembly A6, Component Location Diagram.


PPS X 10¹ (BCD)
PPS X 10⁰ (BCD)
CONT
ON HOOK
OFF HOOK/ DIAL
ID/ PULSE COUNT MIN
MAX
P/O J2
P/O U29
+5V
R55 10K
R32 10K
R31 10K
R45 10K
R46 10K
R59 10K
R58 10K
R48 10K
R49 10K
R50 10K
P/O J1
I/O
MEMR
AB0
AB1
AB2
AB4
AB3
U19A
U20A
U20B
U19B
U19C
G2A/B
G1
U21 74LS138N ADDRESS DECODER
U23A 74S368N TRI-STATE BUS DRIVER
U22
U24A
D0 D1 D2 D3 D4 D5 D6 D7
U18 CD4060 OSC&÷64
C21 39 PF
C20 10 PF
R29 1K
R30 10M
Y1 2.56 MHZ
U17A U17B U17C U17D U17E U17F
U19D
TP4
+VH
U28 7474N D F/F
U1 75451N DRIVERS
R16,100
+12V
C14 2.2
CR7 IN4148
R14 10
T1
CR2 IN4004
CR3 IN4004
R13 10
C2 2.2
CR1 IN4148
R1 100
-12V
+VI
C1 100
ANALOG RCVR AUX ASSY E1260-03-338 -VH
TP1
STRAP
TP2 +IN
TP3 -IN
R11 100K
R5 1K
CR8 IN4148
CR9 IN4148
CR11 IN4148
CR10 IN4148
U7 UA741CV LIMITER
R4 5K CW
R23 1K
VR2 IN748A (3.9V)
R21 100K
R22 10K
U6 UA741CV SCHMITT TRIGGER
CR15 2.4V
C37 0.82
R56 4700
R57 47
U19D
R17 1K
C8 4.7
R2 33K
U4B 9602 5045 CS
(NOT USED)
MON M
OFFICE GND
MON S
-48V
MON E
MEM EN
XMT FF
LOGIC GND
+12V IN
+5V IN
-12V IN
C18 10
C19 0.01
C22 10
C23 0.01
R15 1K
+VH
C24 10
C25 0.01
VR4
C26 1
Q4 MPSA06
U16 MCT2 OPTO ISOLATOR
R26 2200
R47 100K
CR12 IN4148
R27 24K
VR3 IN752A 5.6V
Q3 MPSA06
R25 2200
R42 121K
CR6 IN4148
R10 24.3K
VR1 IN752A 5.6V
U13 MCT2 OPTO ISOLATOR
U10D
R6 510
R7 510
Q1 2N3906
R9 1K
R8 1K
Q2 2N3903



IC	TYPE	PIN +5V	PIN ⏚	PIN +VI	PIN -VI
U1	7545IN	8	4	—	—
U2,U3 U12	7474N	14	7	—	—
U4	9602	16	8	—	—
U5	7401N	14	7	—	—
U6,U7	UA741CV	—	—	7	4
U8	7402N	14	7	—	—
U9	74393N	14	7	—	—
U10,U20	7400N	14	7	—	—

IC	TYPE	PIN +5V	PIN ⏚	PIN +VI	PIN -VI
U11	7414N	14	7	—	—
U13-U16	MCT2	—	—	—	—
U17	CD4069	14	7	—	—
U18	CD4060	16	8	—	—
U19	7404N	14	7	—	—
U21	74LS138N	16	8	—	—
U22-U28	74368N	16	8	—	—

NOTES:
1. ALL RESISTORS ARE 10K, UNLESS OTHERWISE SPECIFIED.
2. RESISTORS IN OHMS, CAPACITORS IN MICROFARADS.
3. ⏚ IS OFFICE GND
   ▽ IS LOGIC GND
4. C3-7, 9-13, 15-16, 27-36 ARE DECOUPLING CAPS BETWEEN +5V AND GROUND FOR TTL PACKAGES

MODEL 1260A	
REF DES	C1260-03-022
PT NO	A6
PO NO	97011

Figure 6—22. 1260A Analog Receiver Assembly A6, Schematic Diagram.

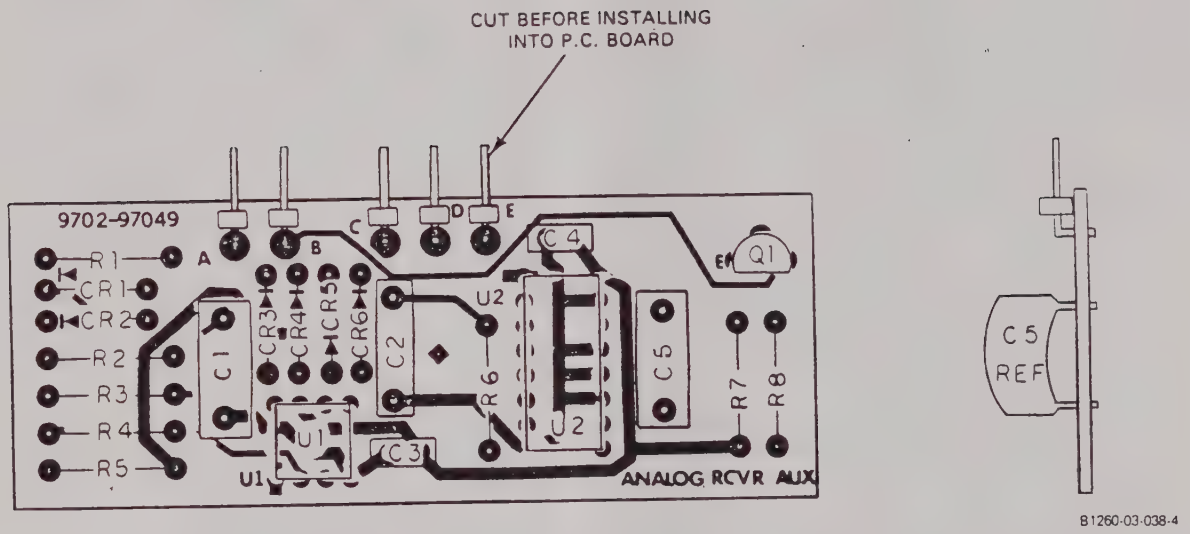


Figure 6—23. 1260A Analog Receiver Auxiliary Assembly Component Location Diagram.

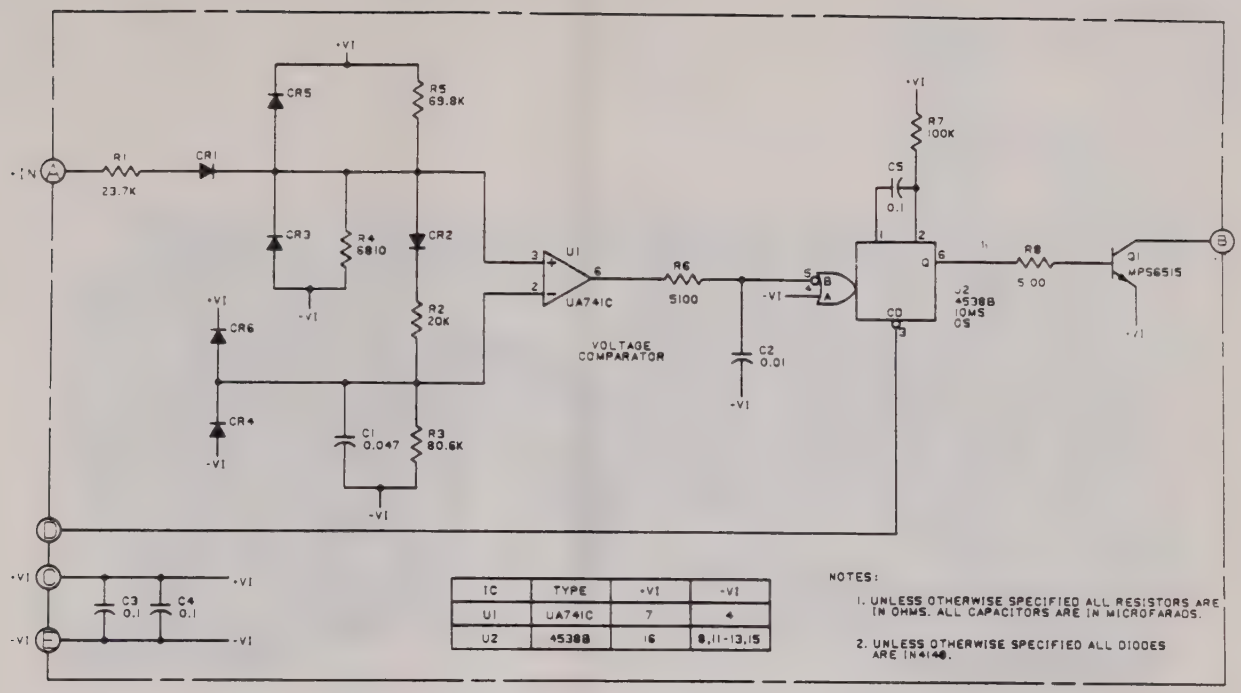


Figure 6—24. 1260A Analog Receiver Auxiliary Assembly Schematic Diagram.

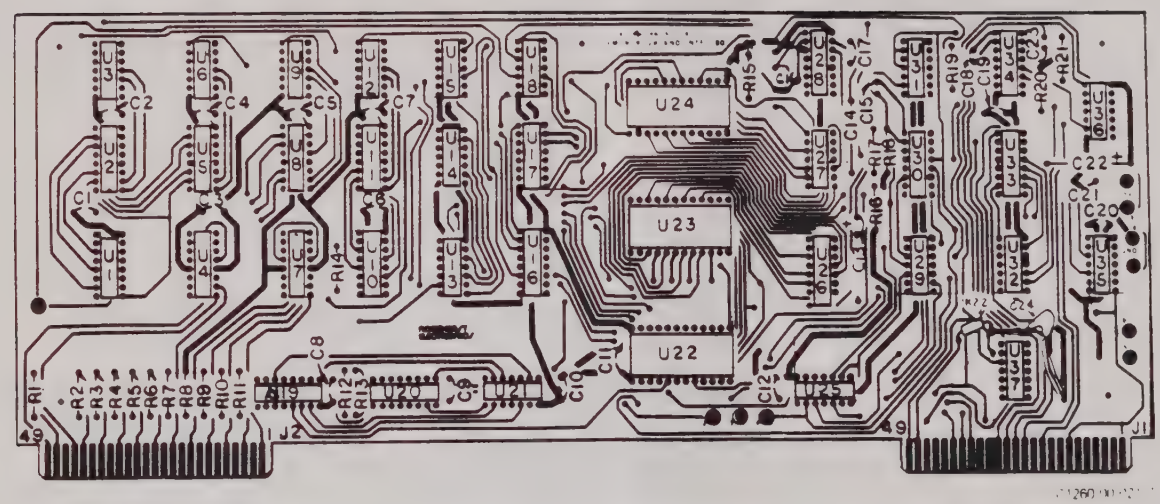
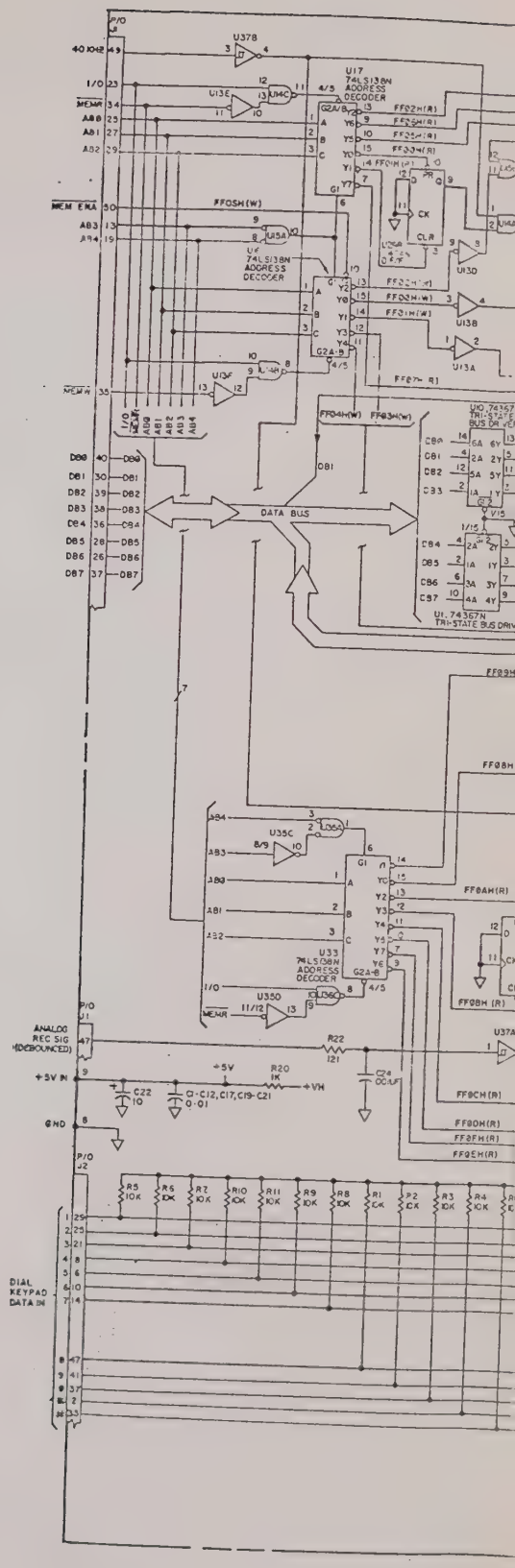
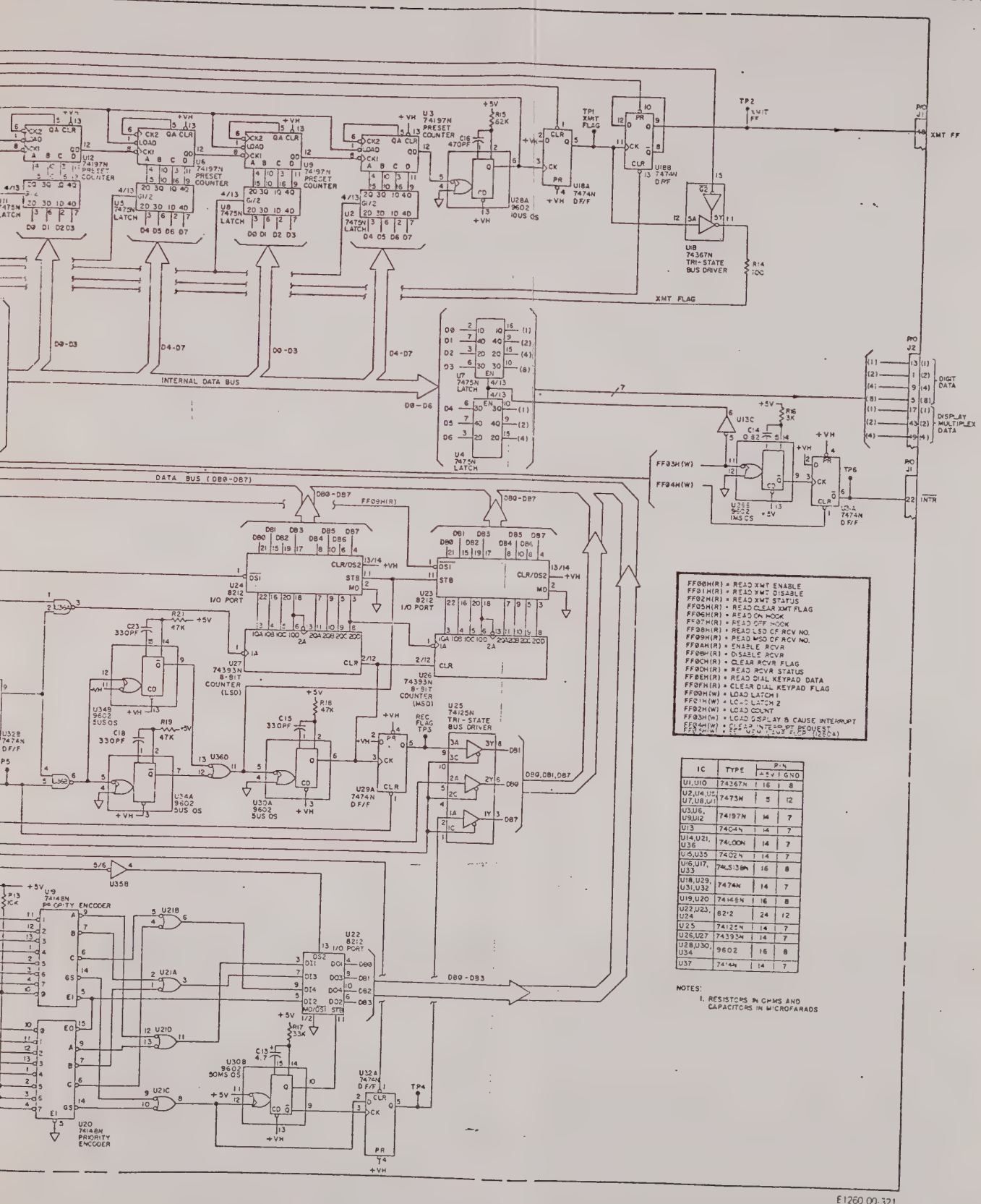


Figure 6—25. 1260A Transmitter, Receiver, and Interface Assembly A7, Component Location Diagram.


DATA BUS
U17 74LS138N ADDRESS DECODER
U6 74LS138N ADDRESS DECODER
U33 74LS138N ADDRESS DECODER
U10,74367 TRI-STATE BUS DRIVER
U1, 74367N TRI-STATE BUS DRIVER
ANALOG REC SIG (DEBOUNCED)
DIAL KEYPAD DATA IN
+5V IN
GND
+5V
+VH
R22 121
R20 1K
C22 10
C24 .001uF
FF02H(R)
FF03H(R)
FF04H(R)
FF05H(R)
FF06H(R)
FF07H(R)
FF08H(R)
FF0AH(R)
FF0CH(R)
FF0DH(R)
FF0EH(R)
FF0FH(R)
FF05H(W)
FF03H(W)
FF04H(W)
FF01H(W)


INTERNAL DATA BUS
DATA BUS (D80-D87)
D80-D87
D80-D83
D84-D87
XMT FLAG
XMT FF
INTR
DIGIT DATA
DISPLAY MULTIPLEX DATA
FF00H(R) = READ XMT ENABLE
FF01H(R) = READ XMT DISABLE
FF02H(R) = READ XMT STATUS
FF05H(R) = READ CLEAR XMT FLAG
FF06H(R) = READ ON HOOK
FF07H(R) = READ OFF HOOK
FF08H(R) = READ LSD OF RCV NO.
FF09H(R) = READ MSD OF RCV NO.
FF0AH(R) = ENABLE RCVR
FF0BH(R) = DISABLE RCVR
FF0CH(R) = CLEAR RCVR FLAG
FF0DH(R) = READ RCVR STATUS
FF0EH(R) = READ DIAL KEYPAD DATA
FF0FH(R) = CLEAR DIAL KEYPAD FLAG
FF00H(W) = LOAD LATCH 1
FF01H(W) = LOAD LATCH 2
FF02H(W) = LOAD COUNT
FF03H(W) = LOAD DISPLAY & CAUSE INTERRUPT
FF04H(W) = CLEAR INTERRUPT REQUEST
FF05H(W) = SET NEW TWO FLIP (USED)

IC	TYPE	PIN +5V	PIN GND
U1, U10	74367N	16	8
U2, U4, U6, U7, U8, U11	7475N	5	12
U3, U5, U9, U12	74197N	16	7
U13	7404N	14	7
U14, U21, U36	7400N	14	7
U15, U35	7402N	14	7
U16, U17, U33	74LS138N	16	8
U18, U29, U31, U32	7474N	14	7
U19, U20	74148N	16	8
U22, U23, U24	8212	24	12
U25	74125N	14	7
U26, U27	74393N	14	7
U28, U30, U34	9602	16	8
U37	7414N	14	7

NOTES:
1. RESISTORS IN OHMS AND CAPACITORS IN MICROFARADS

E1260 09-321

Figure 6—26. 1260A Transmitter, Receiver, and Interface Assembly A7, Schematic Diagram.

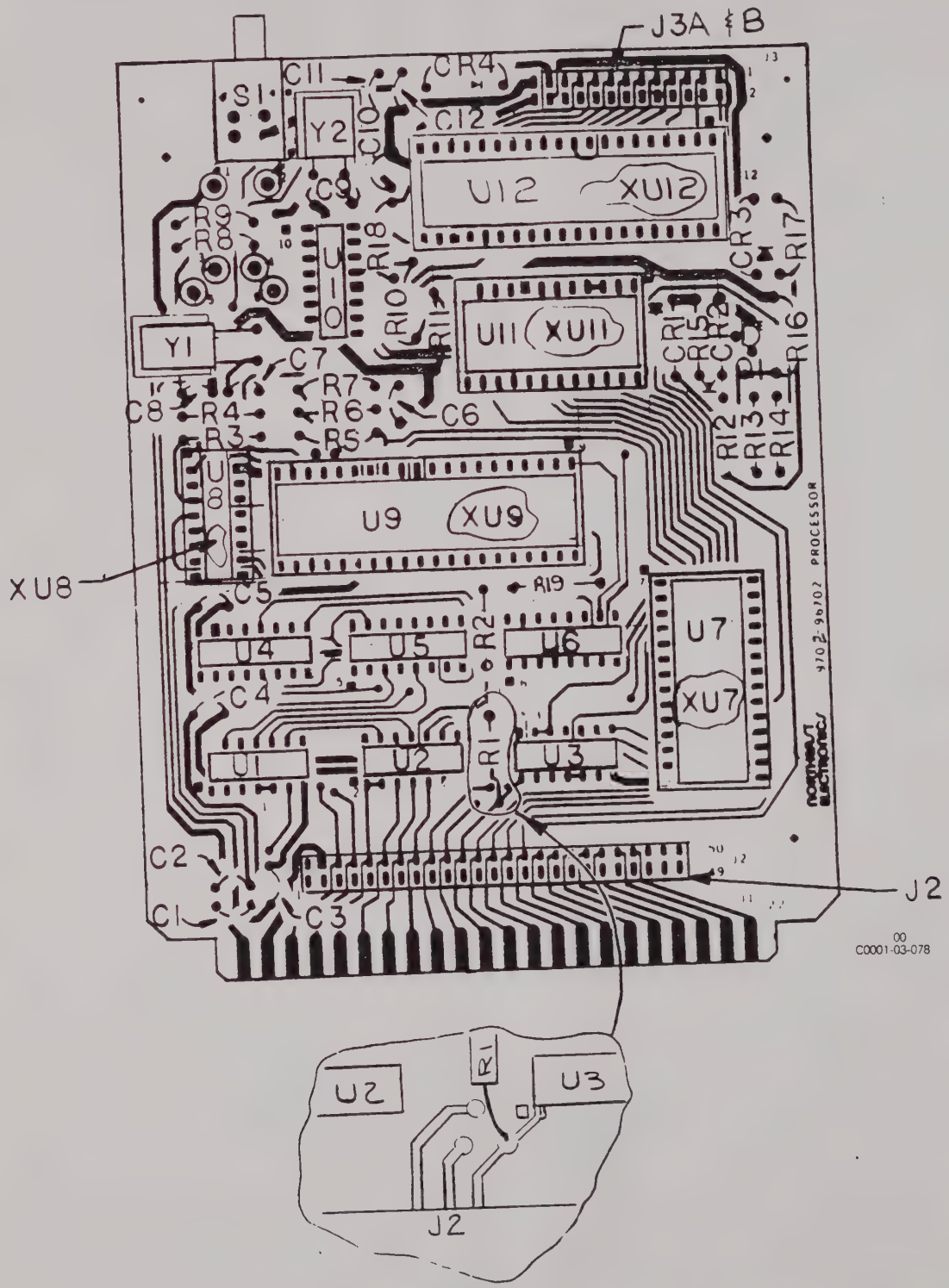
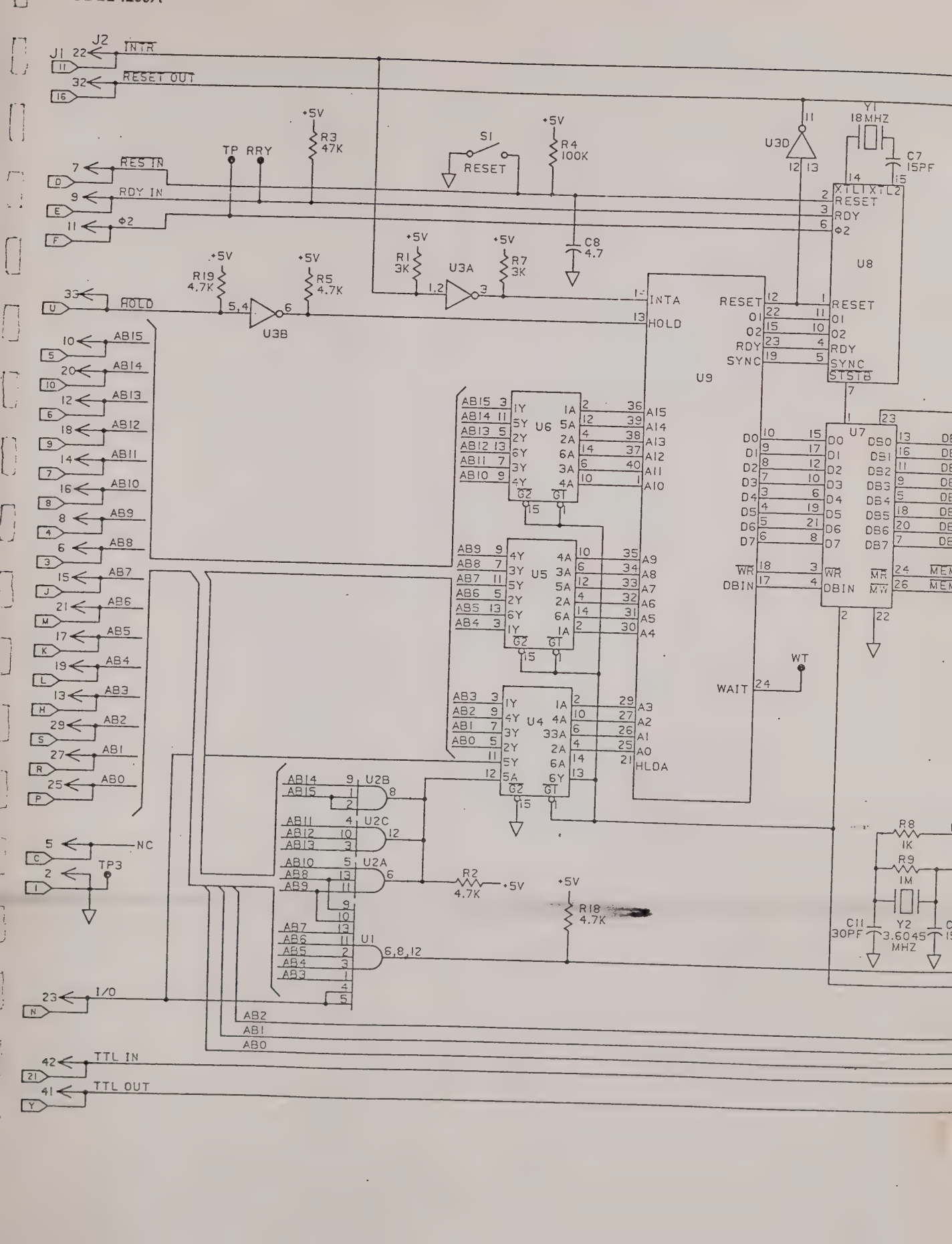


Figure 6—27. 1260A CPU Assembly A8, Component Location Diagram.


J2
INTR
RESET OUT
J1
TP RRY
+5V
R3 47K
RES IN
RDY IN
Φ2
S1
RESET
R4 100K
C8 4.7
R1 3K
U3A
R7 3K
R19 4.7K
R5 4.7K
U3B
HOLD
U3D
Y1 18MHZ
C7 15PF
XTL1 XTL2
RESET
RDY
Φ2
U8
INTA
HOLD
RESET
O1
O2
RDY
SYNC
STSTB
U9
U6
U5
U4
AB15
AB14
AB13
AB12
AB11
AB10
AB9
AB8
AB7
AB6
AB5
AB4
AB3
AB2
AB1
AB0
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
HLDA
U7
D0
D1
D2
D3
D4
D5
D6
D7
WR
DBIN
WT
WAIT
U2B
U2C
U2A
U1
R2 4.7K
R18 4.7K
R8 1K
R9 1M
C11 30PF
Y2 3.6045 MHZ
NC
TP3
I/O
TTL IN
TTL OUT

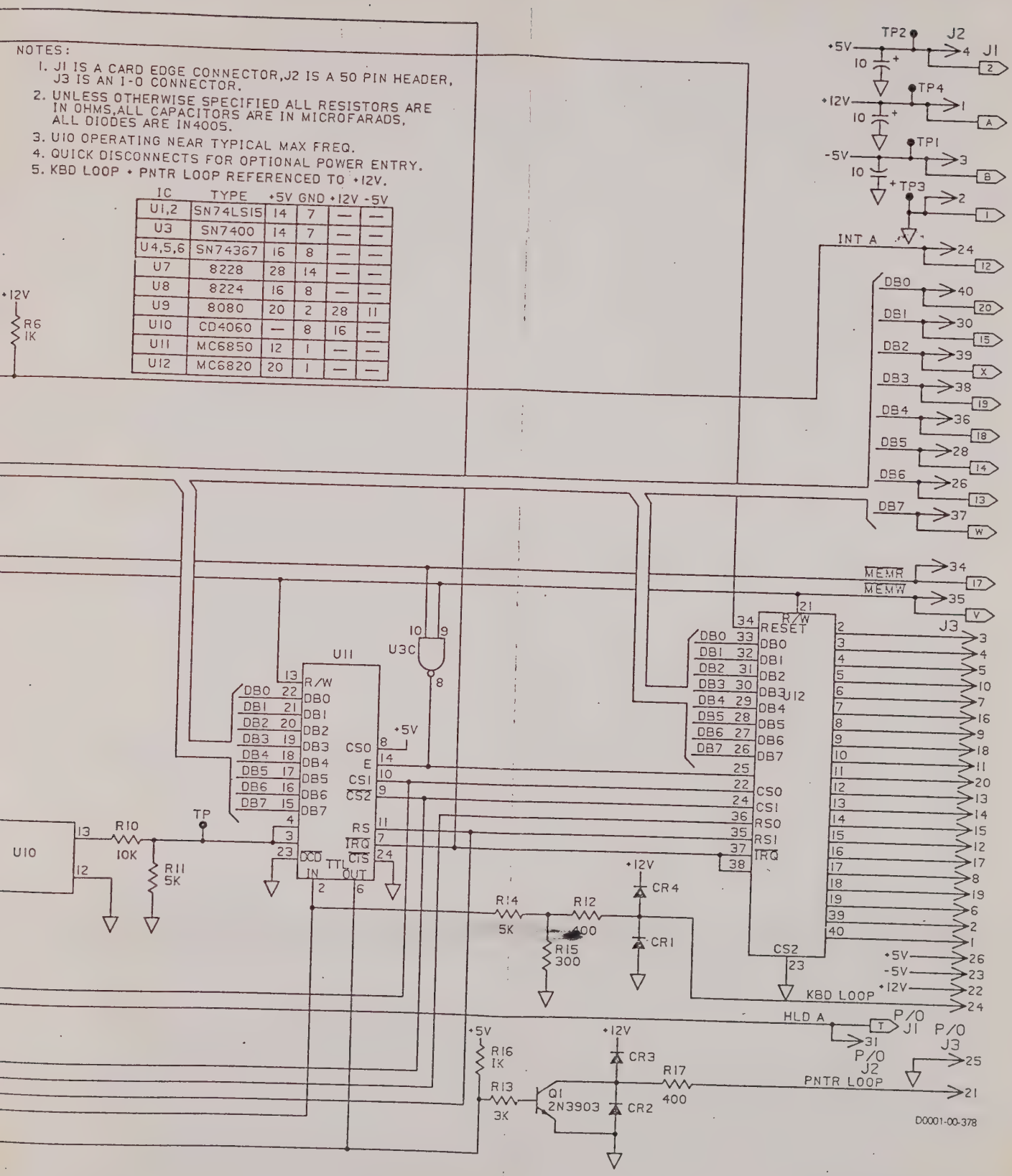


Figure 6—28. 1260A CPU Assembly A8, Schematic Diagram.

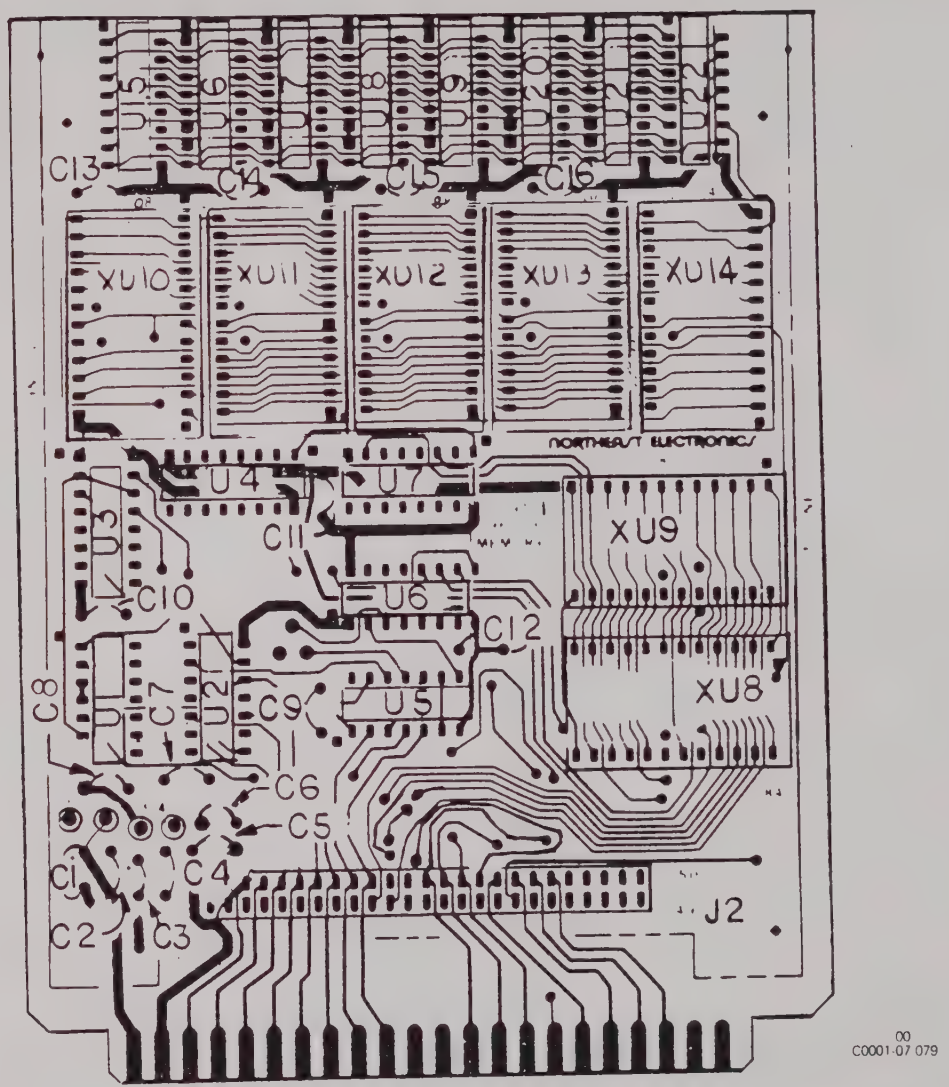
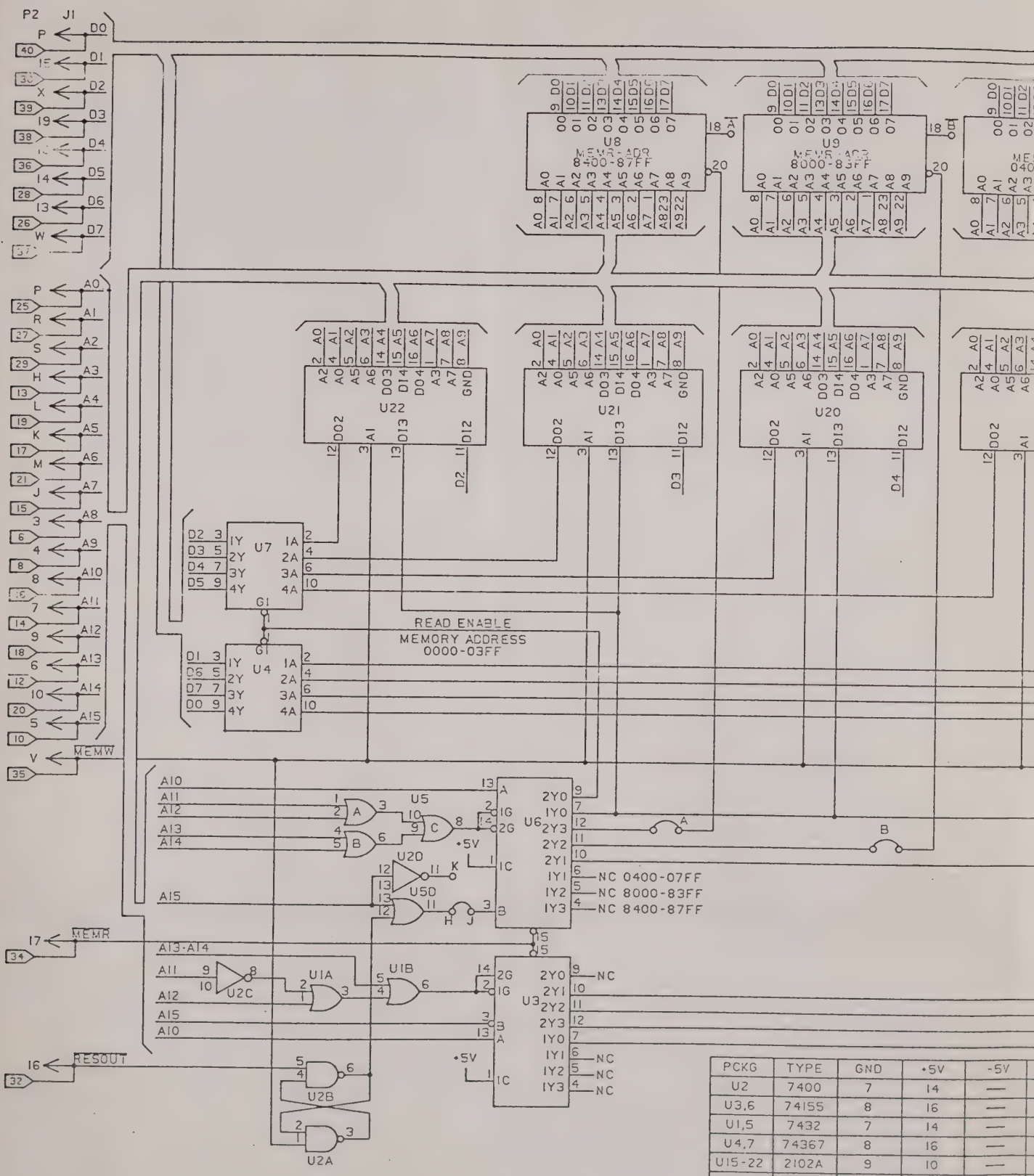
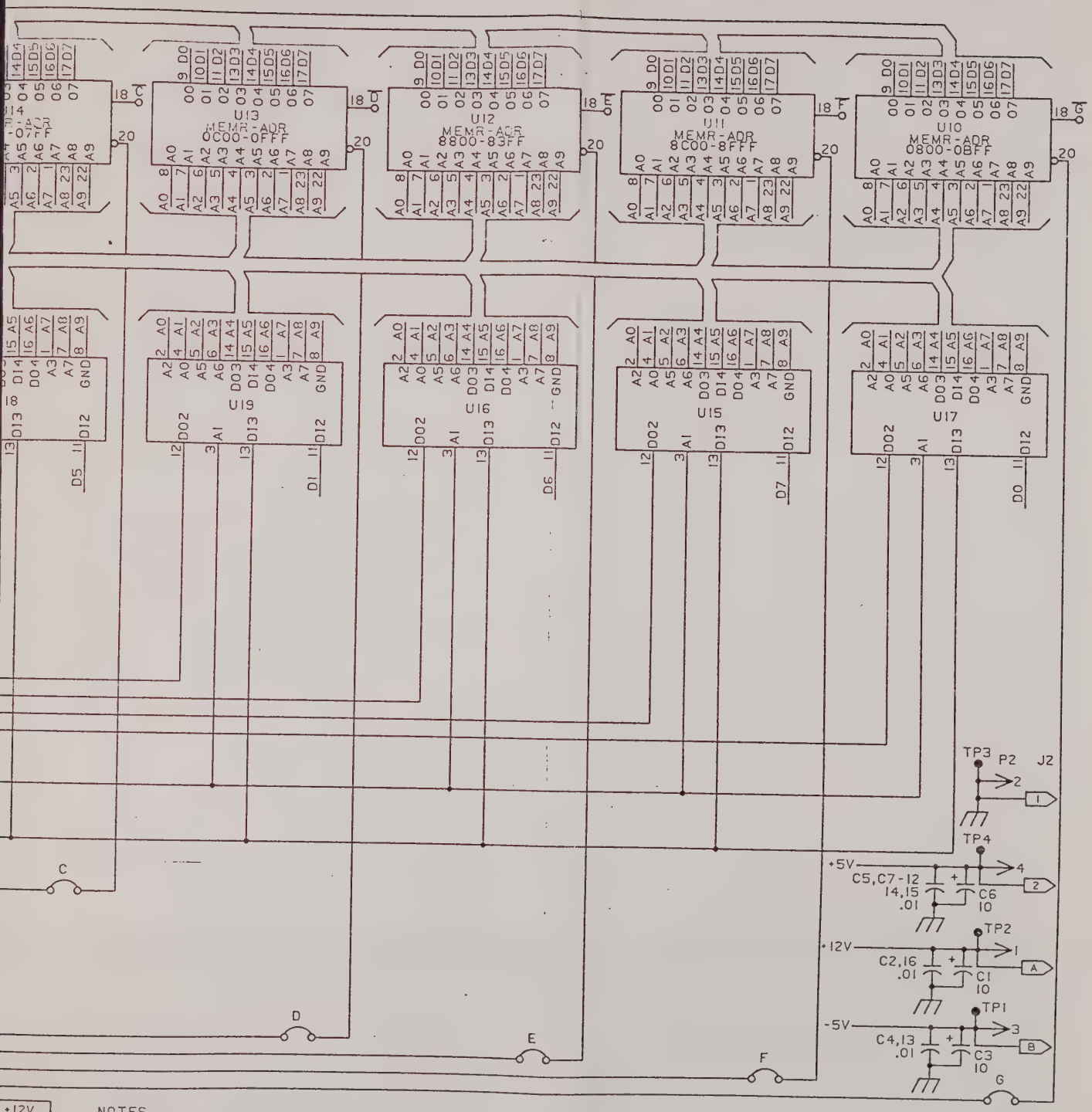


Figure 6—29. 1260A Memory Assembly A9, Component Location Diagram.



PCKG	TYPE	GND	+5V	-5V
U2	7400	7	14	—
U3,6	74155	8	16	—
U1,5	7432	7	14	—
U4,7	74367	8	16	—
U15-22	2102A	9	10	—
U8-14	8708	12	24	21

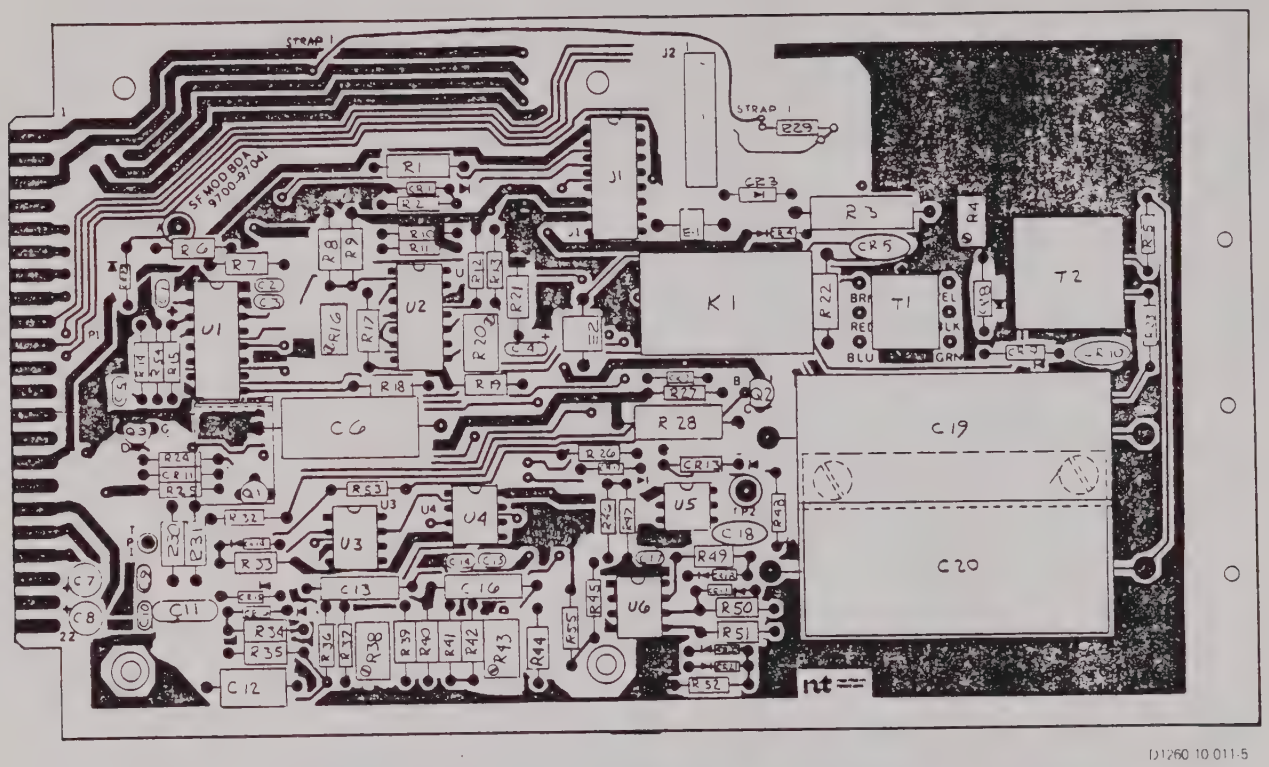


NOTES

1. UNLESS OTHERWISE SPECIFIED:
   - -CAPACITORS ARE IN MICROFARADS
   - -RESISTORS ARE IN OHMS
   - -RESISTORS ARE 1/4W 10%
   - -DIODES ARE IN4148

D0001-00-379

Figure 6—30. 1260A Memory Assembly A9, Schematic Diagram.



D1260 10 011-5

Figure 6—31. SF Adapter Option 1260-10 Board A Component Location Diagram.

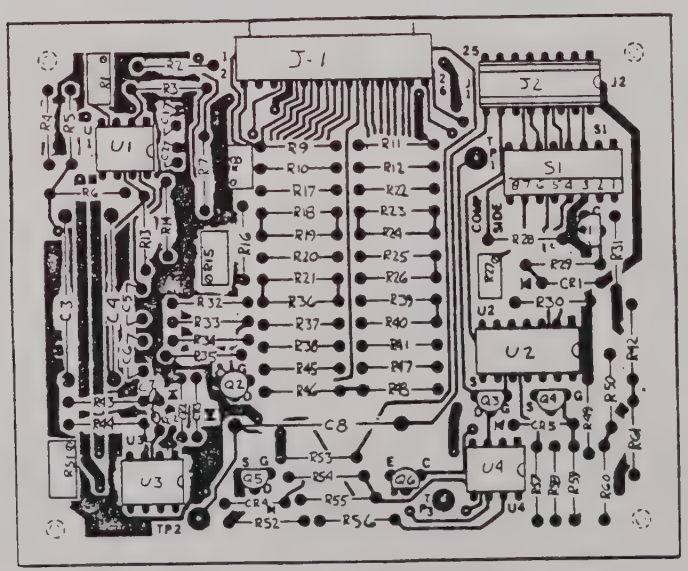
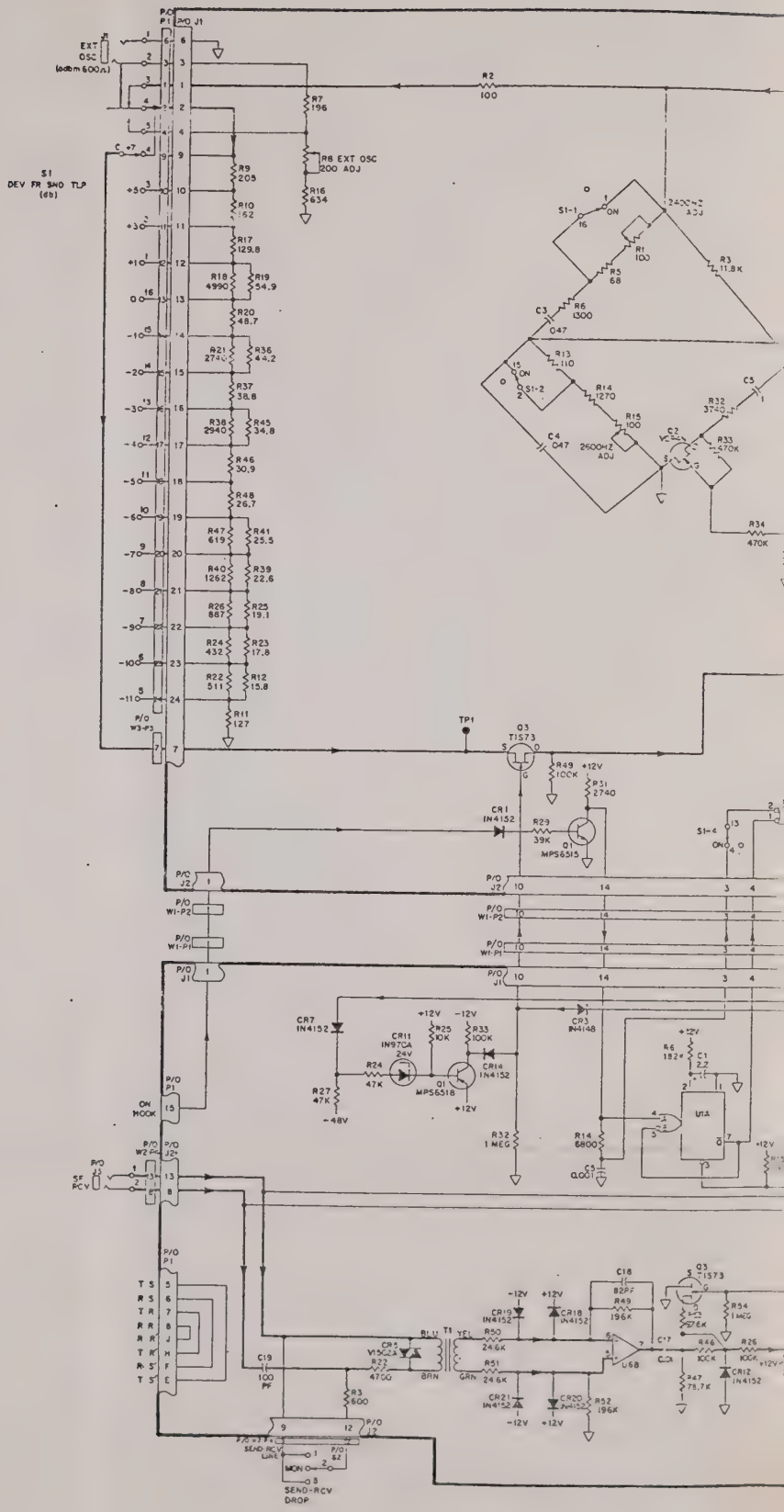


Figure 6—32. SF Adapter Option 1260-10 Board B Component Location Diagram.


P/O P1
P/O J1
EXT OSC
(600Ω)
R2 100
R7 196
R8 EXT OSC 200 ADJ
R16 634
S1 DEV FR SHO TLP (db)
R9 205
R10 152
R17 129.8
R18 4990
R19 54.9
R20 48.7
R21 2740
R36 44.2
R37 38.8
R38 2940
R45 34.8
R46 30.9
R48 26.7
R47 619
R41 25.5
R40 1262
R39 22.6
R26 887
R25 19.1
R24 432
R23 17.8
R22 511
R12 15.8
R11 127
P/O W3-P3
TP1
Q3 T1S73
R49 100K
+12V
P31 2740
CR1 IN4152
R29 39K
Q1 MPS6515
S1-4
P/O J2
P/O W1-P2
P/O W1-P1
P/O J1
CR7 IN4152
CR11 IN970A 24V
R24 47K
R27 47K
-48V
+12V
-12V
R25 10K
R33 100K
CR14 IN4152
Q1 MPS6518
CR3 IN4148
R6 182K
C1 2.2
U1A
R14 6800
C5 0.01
R32 1 MEG
ON HOOK
P/O P1
P/O J2
SF RCV
P/O W2-P2
P/O P1
T S
R S
T R
R R
R T
T S'
R S'
T S'
C19 100 PF
R3 600
P/O J2
SEND RCV LINE
MON
SEND-RCV DROP
C18 82PF
R49 196K
CR19 IN4152
CR18 IN4152
R50 24.6K
R51 24.6K
CR21 IN4152
CR20 IN4152
R52 196K
T1
YEL
BLU
GRN
BRN
CR4 V150LA2
R22 470Ω
C17
U6B
R44 100K
R26 100K
R47 78.7K
CR12 IN4152
R54 1 MEG
Q3 T1S73
1240Hz ADJ
S1-1
R1 100
R5 68
R3 11.8K
C3 .047
R6 1300
R13 110
S1-2
R14 1270
R15 100
2600Hz ADJ
C4 .047
C2
R33 470K
R32 3740
C5
R34 470K

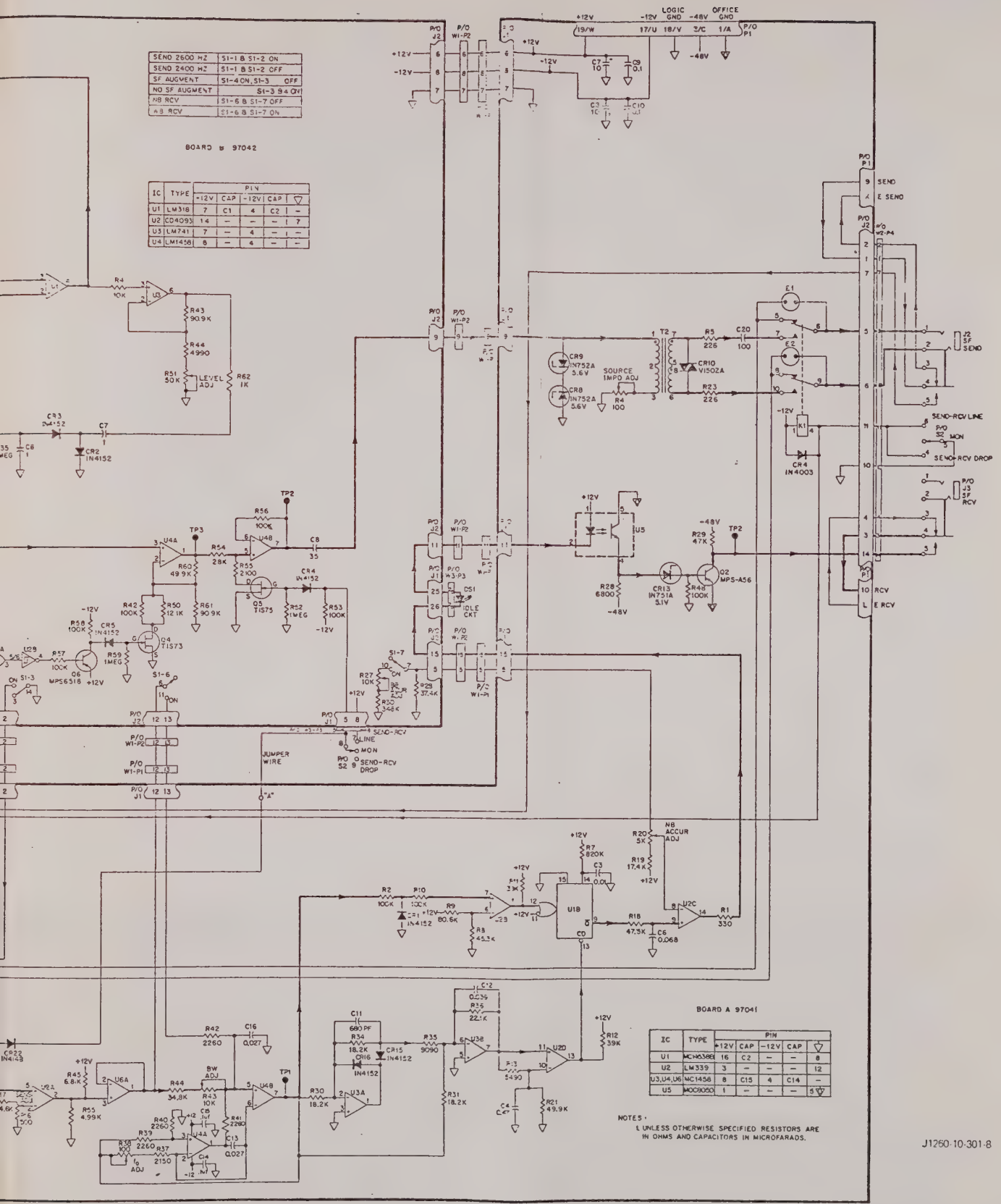
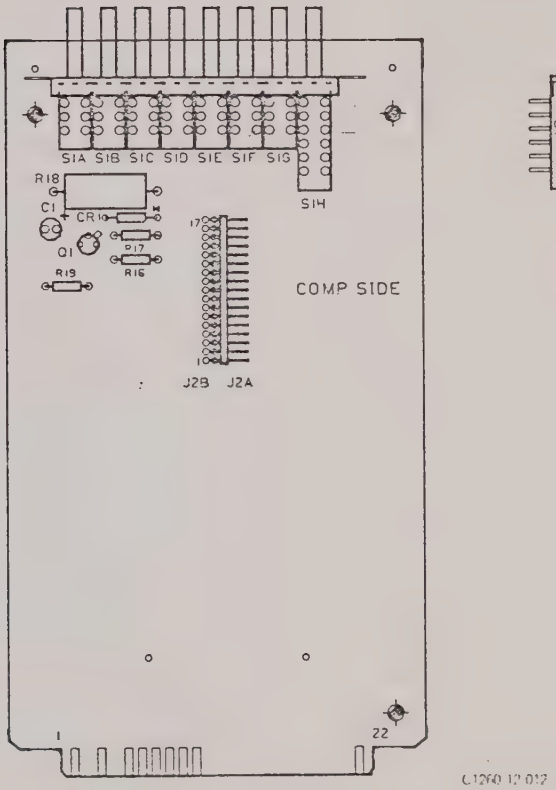


Figure 6—33. SF Adapter Option 1260-10 Schematic Diagram.



ARTLINE MODULE 97090

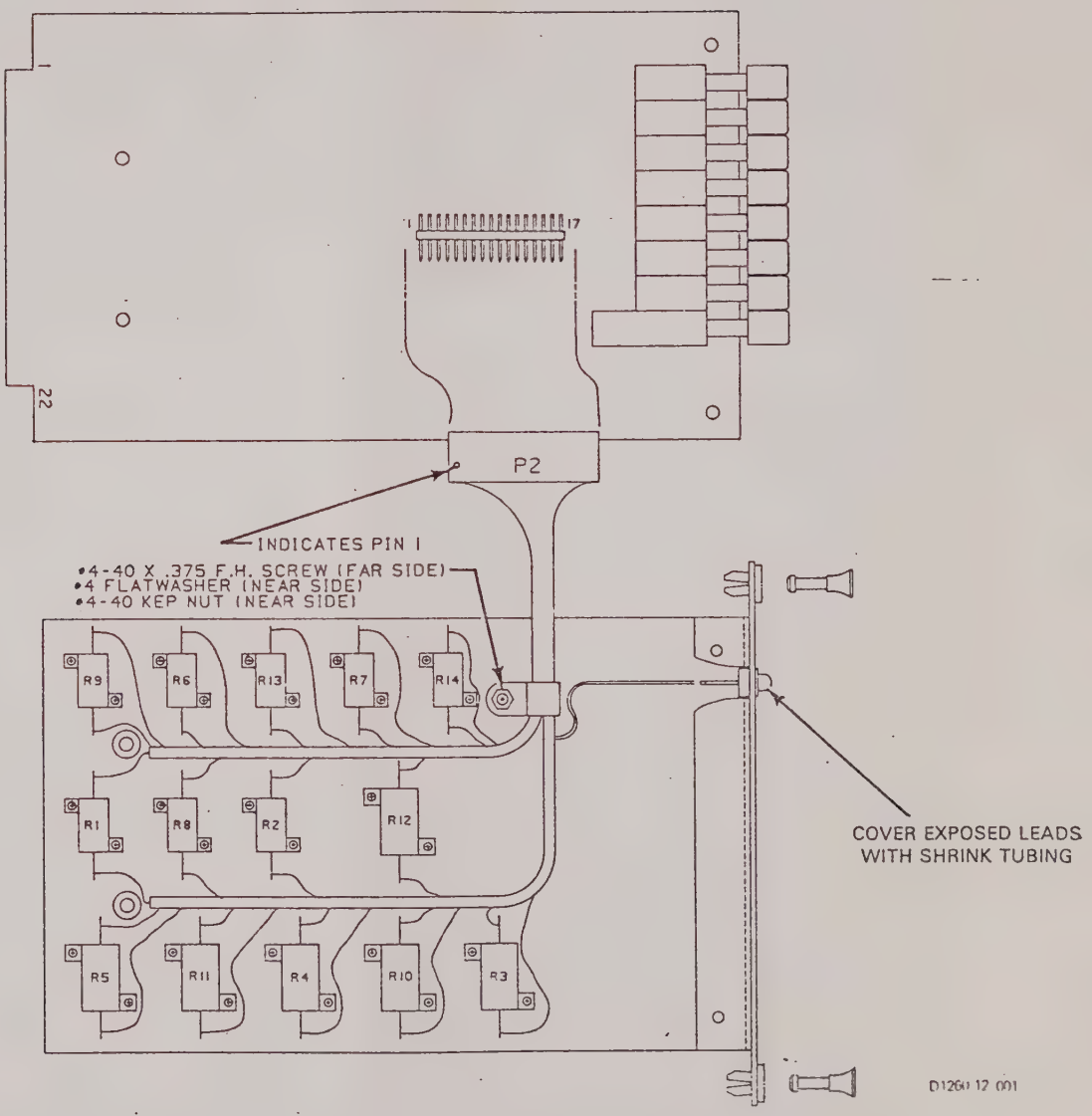
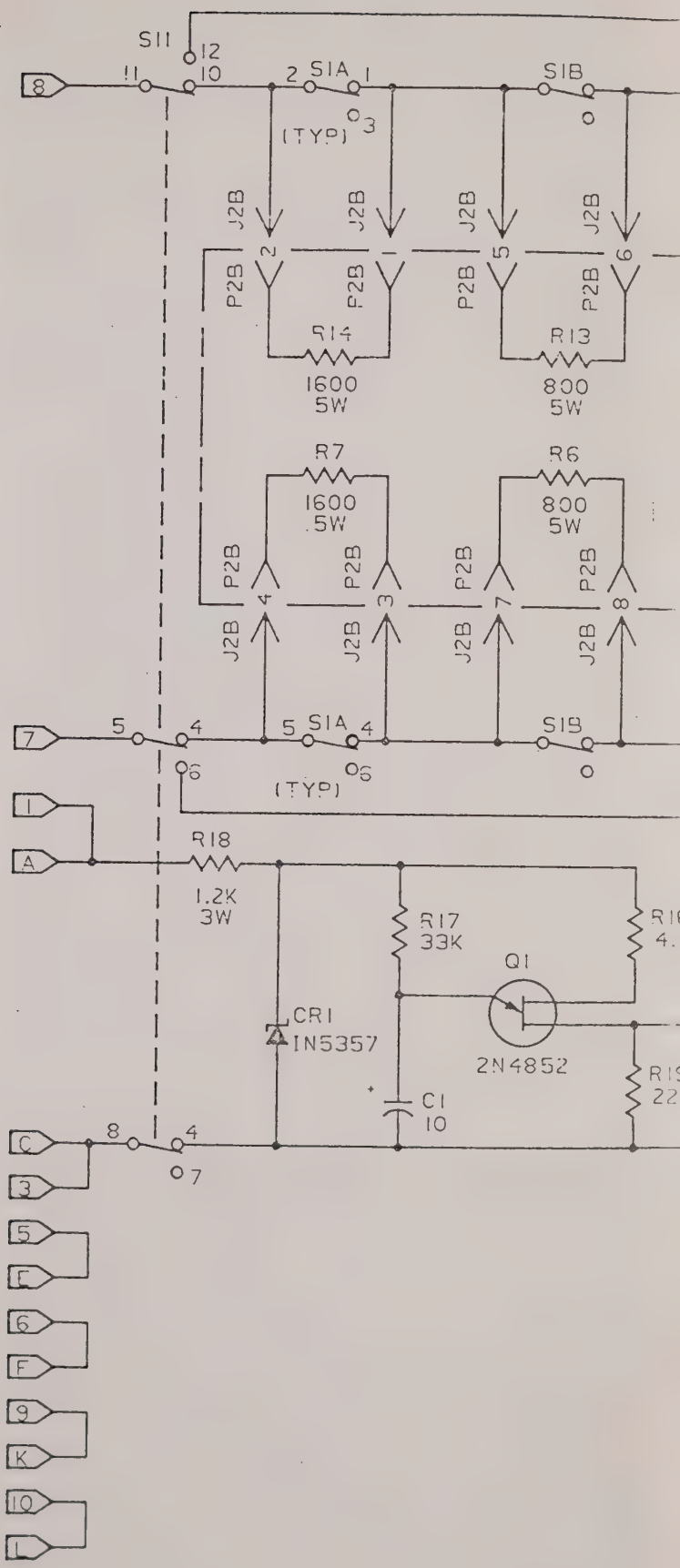
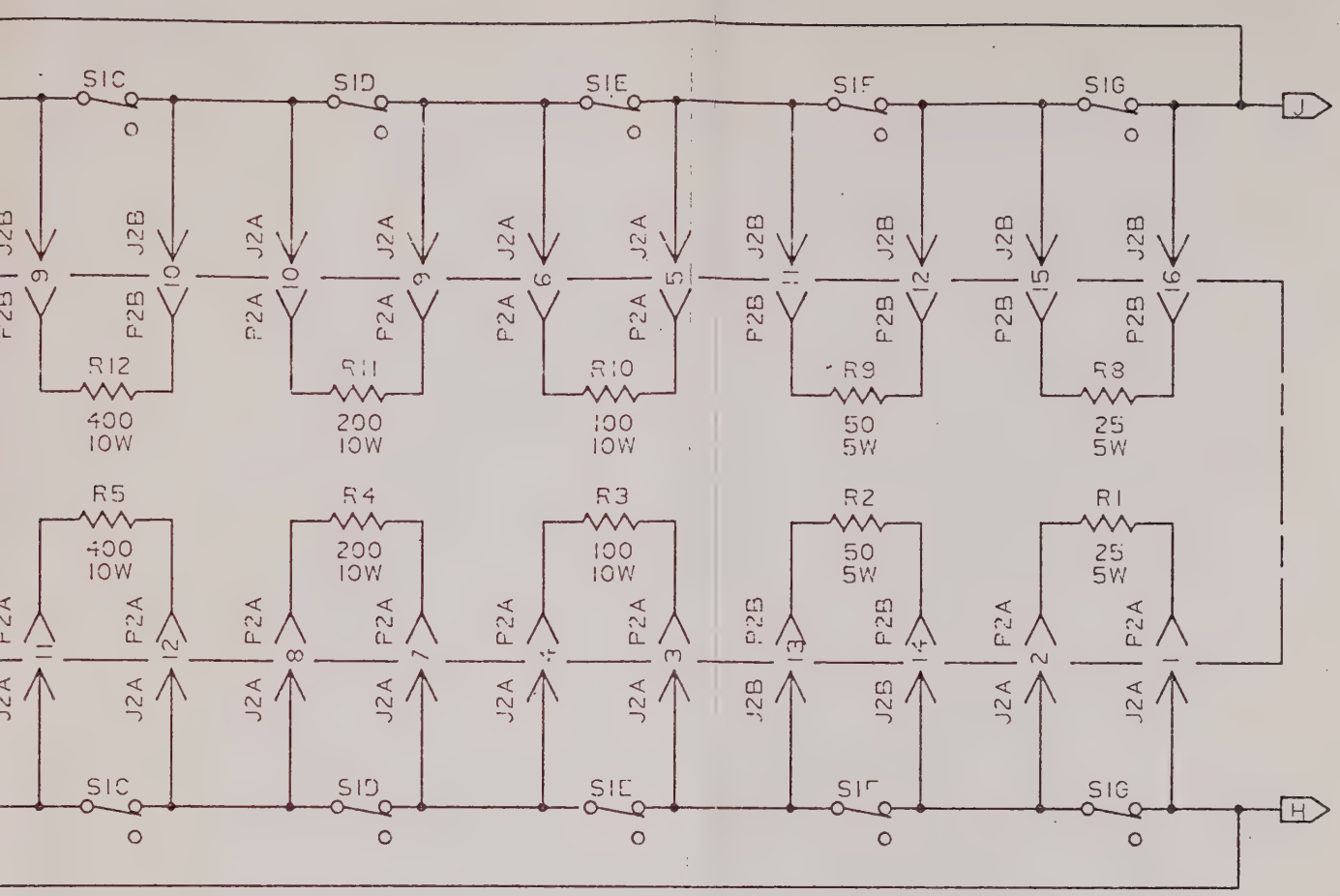
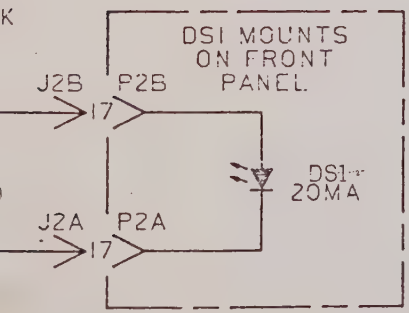


Figure 6—34. Local Pulse Repeating Artline Option 1260-12 Component Location Diagram.


S11
12
10
11
8
2
S1A
1
3
(TYP)
S1B
J2B
P2B
2
1
5
6
R14
1600
5W
R13
800
5W
R7
1600
5W
R6
800
5W
4
3
7
8
5
4
6
7
I
A
R18
1.2K
3W
R17
33K
Q1
2N4852
CR1
IN5357
C1
10
C
3
5
F
6
F
9
K
10
L





NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTORS ARE 1/4W, 10%.
2. UNLESS OTHERWISE SPECIFIED CAPACITORS ARE IN MICROFARADS.

C1260 12 312-1

Figure 6—35. Local Pulse Repeating Artline Option 1260-12 Schematic Diagram.

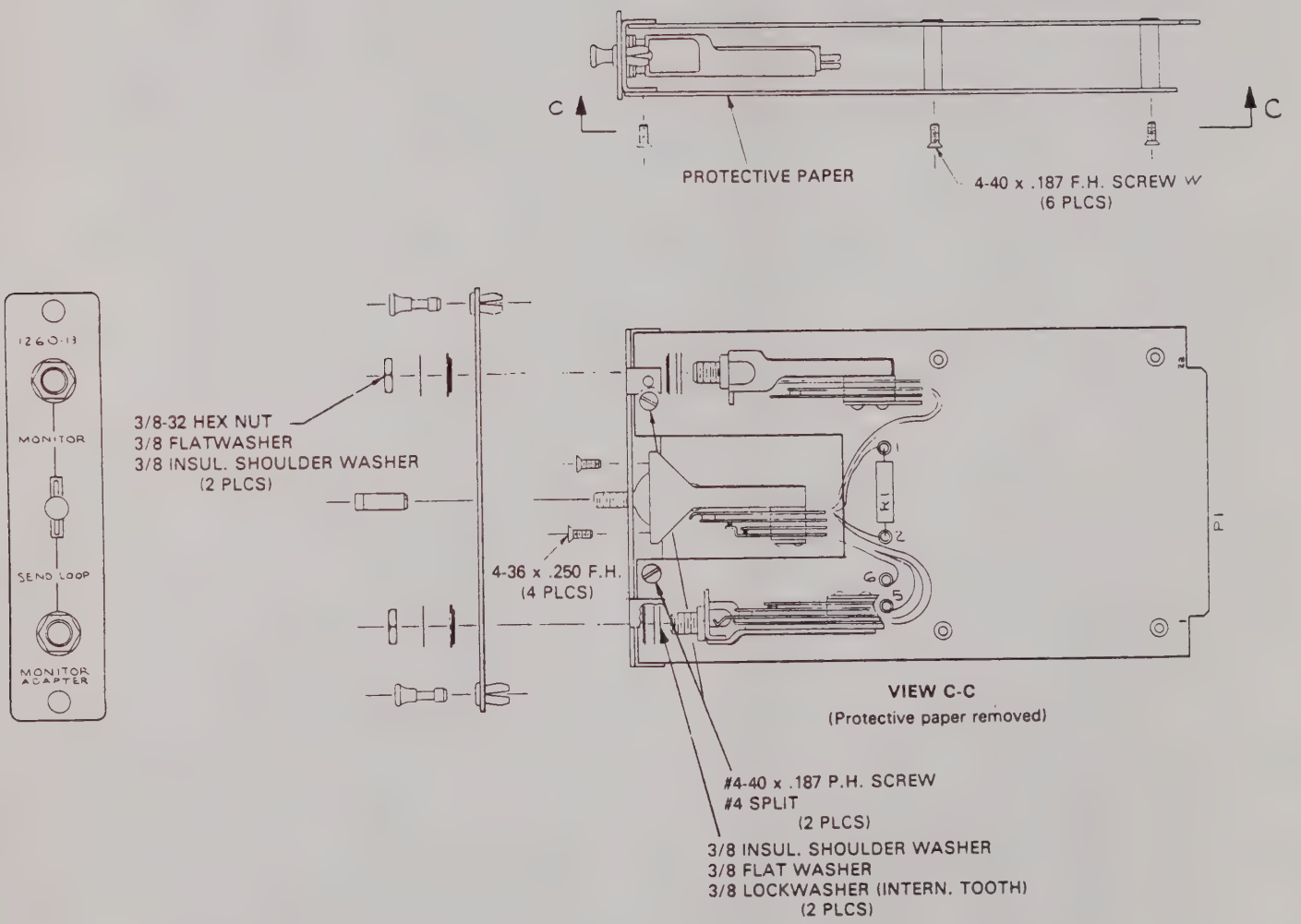


Figure 6—36. Monitor Adapter Option 1260-13 Component Location Diagram.

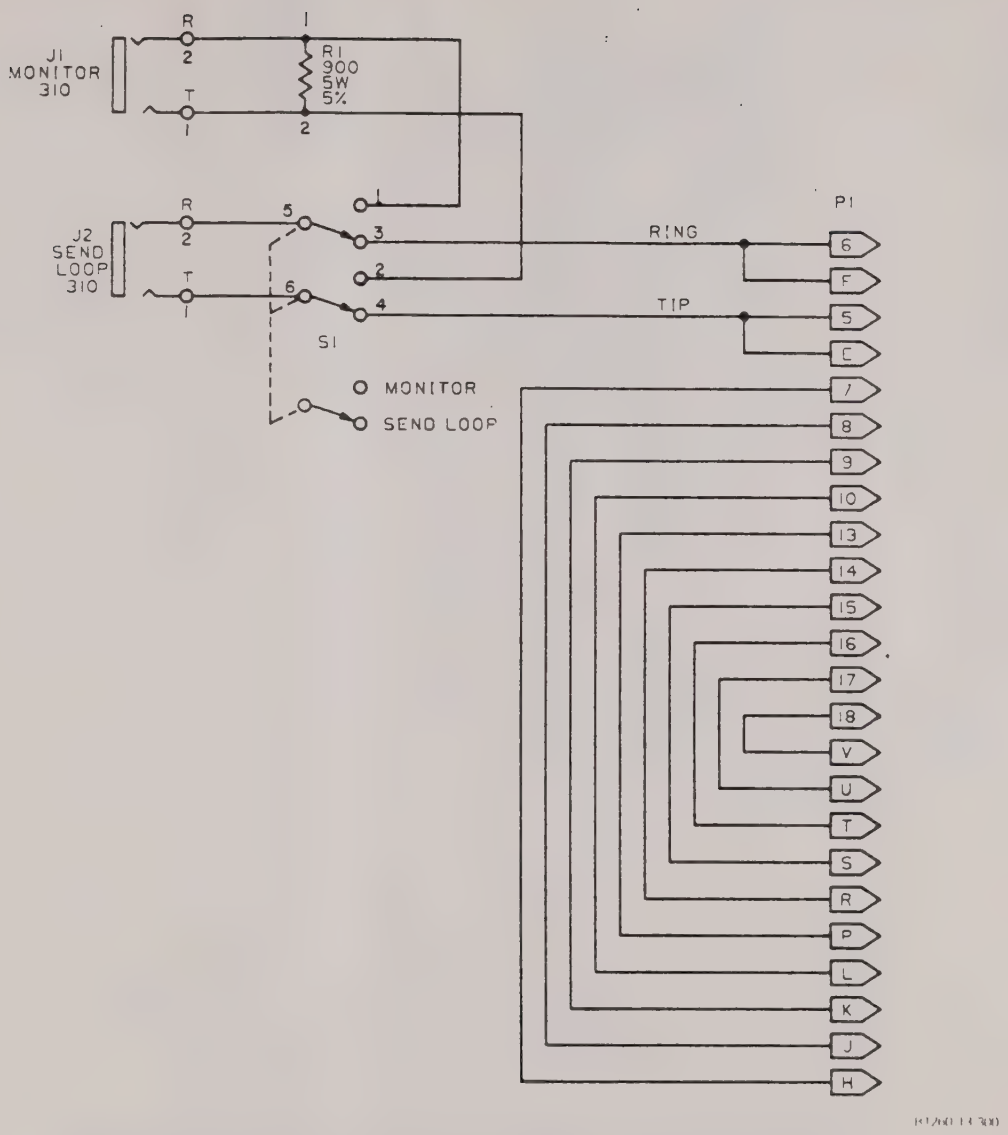


Figure 6—37. Monitor Adapter Option 1260-13 Schematic Diagram.

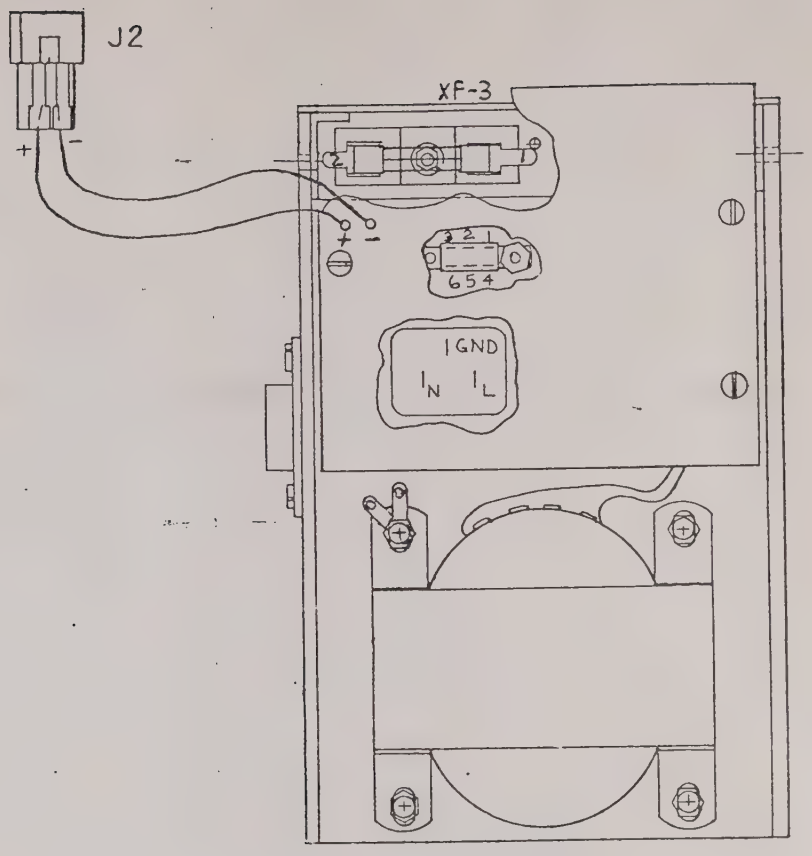
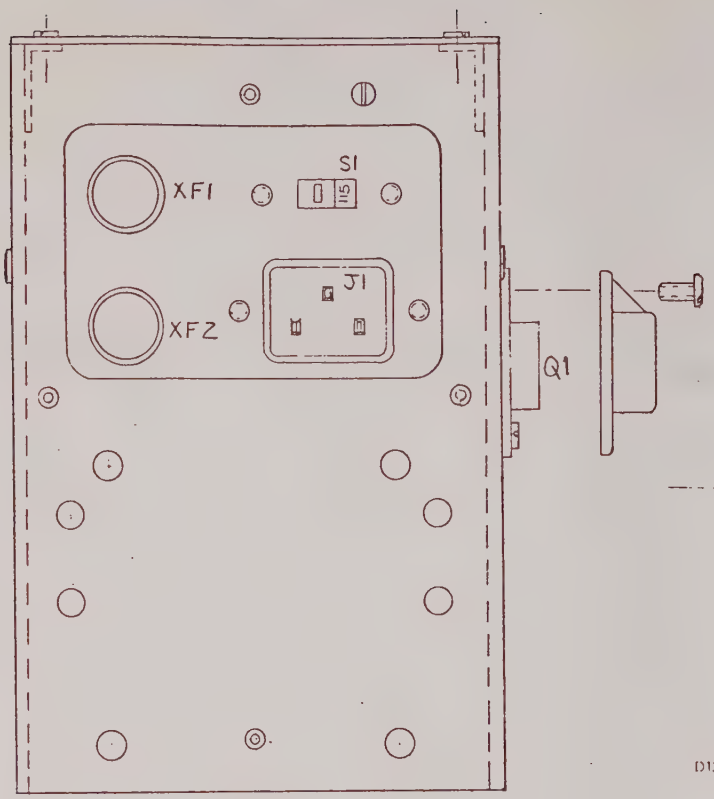
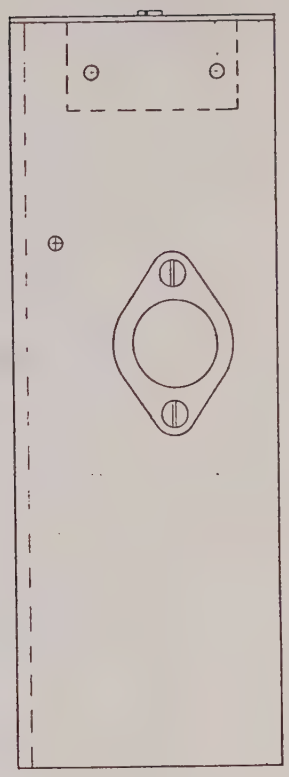


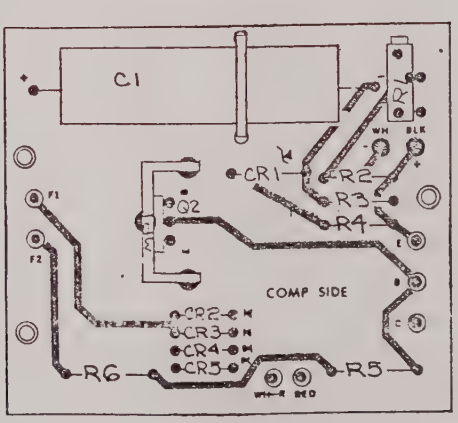
Figure 6—38. AC Power Supply Option 1260-11 Component Location Diagram.



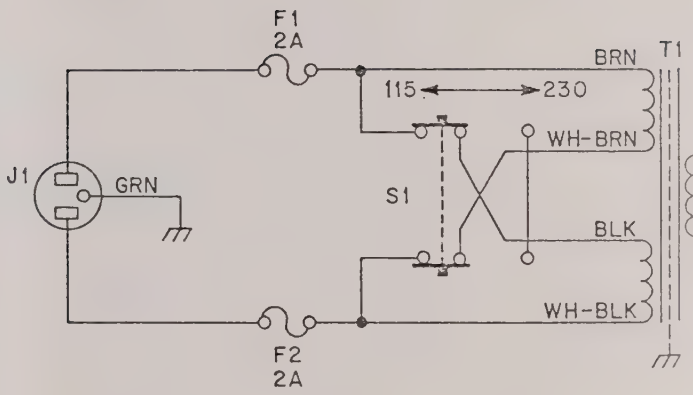
FRONT VIEW



SIDE VIEW

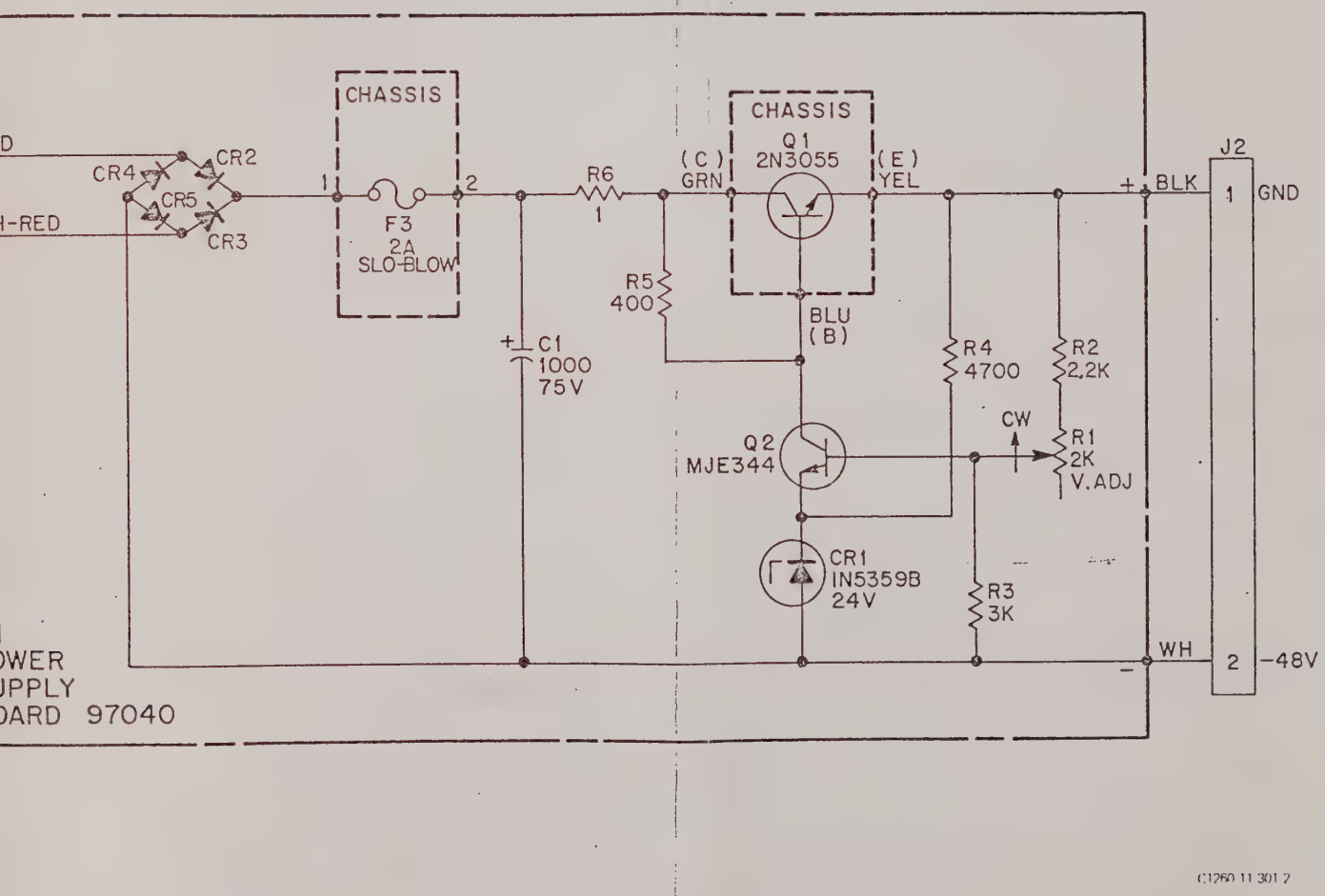


B1260 11 011 2



NOTES:

1. UNLESS OTHERWISE NOTED, ALL DIODES ARE IN4005.



C1260 11 301 2

Figure 6—38. AC Power Supply Option 1260-11 Schematic Diagram.

SECTION 7

ELECTRONIC PARTS LIST

7.1 This section contains the electronic parts lists for the Model 1260A.

Table 7—1. Model 1260A Front and Rear Panel Assemblies Overall Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
A11	FRONT PNL ASSY 1260A		A126003024
A12	REAR PNL ASSY 1260A		A126003025
J3	CONN HSNG,FEMALE 2P W/O	2 PIN	650910102
J6	JACK,TEL,SWCRFT SCHEM 4		650100300
W2	DISPLAY CABLE W2		A126000012
W3	THUMBWHEEL CABLE W3		A126000013

Table 7—2. Model 1260A Front Panel Assembly A11 Overall Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
A1	1260A SUPPRESSOR BD A1		A126003015
A2	1260A DISPLAY BD A2		A126003016
A3	LOOP RES.&LAMP 96752 A3		A126000017
A4	LINE LEAK 96751 A4		A126000019
A5	THUMBWHEEL A5 PC 97007		A126003018
C1	CAPACITR POLYESTR 150 NF	CAP.045 N 400V 10%	320001545
DS1-5	DIODE LED-RED		564500802
J2	BINDING POST METAL GND		652500100
M1	METER,26D	1 MA	900000001
R1	RESISTOR CARBON 3.3 K	RES.003 N 1/2W 5%	200203325
R2	R2 MOD		A126003209
R3	RESISTOR WIREOW 400 R	25W 5%	210904017
R7	RESISTOR CARBON 330 R	RES.003 P 1/2W 10%	200203316
S1	CIRCUIT BKR,WITH LED IND.	2.5 A	862901201
S2	SWITCH,PB MOM.	SPST N.C.	635500202
S3-4	SWITCH,PB MOM.	SPST	635500201
S17	12 BUTTON KEYPAD		635000300
S18	1260A STRAP. DIAGRAM S18		A126003037
S19	1260A RCV SWITCH ASSY S19		A126003026
S20	1260A SND SWITCH ASSY S20		A126003027
S21	2C-2C CONTACT		630100601
S22	ON-NONE-ON	SPDT 5A 28V	620400100

Table 7—3. Model 1260A Suppressor Assembly A11A1 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
J1-4	JACK,TEL,SCHEM.4,PC PINS	HI-D	650101800
J5-6	HEDR,PC BD TO CONN	7 SIL	654003429
RV1-8	VARISTOR V95LA		565500201

Table 7—4. Model 1260A Display Assembly A11A2 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
C1	CAPACITR CERAMIC 10 NF	CAP.093 50V 00 Z5V	330701030
CR1-2	DIODE SIGNAL 1N4148	DIO.001 75V SI 4.0NS	560041480
J2	HEDR,PC BD TO CONN	13 SIL	654003423
Q1-6	TRANSSTR BJT-PNP MPS6534	TO92.01 40V SI HFE90 600MA	552065340
Q7	TRANSSTR BJT-NPN MPS6515	TO92.01 25V SI HFE250 0.1A	550065150
R1-6	RESISTOR CARBON 1.0 K	RES.001 P 1/4W 10%	200101026
R7	RESISTOR CARBON 2.2 K	RES.001 P 1/4W 10%	200102226
R8	RESISTOR CARBON 10 K	RES.001 P 1/4W 10%	200101036
R9	RESISTOR CARBON 1.0 K	RES.001 P 1/4W 10%	200101026
R10-19	RESISTOR CARBON 120 R	RES.001 P 1/4W 10%	200101216
U1-5	READOUT 7SEG.HIGH EFF..43	14PDIL 20MA RED	728301701
U6	HIGH EFF 7 SEG .43IN RHDP	14DIP RED	728301704
U7	INT-CKT LS-TTL 74LS138	DIP.16 P 3-8 LINE DEC/DEMUX	510974138
U8	INT-CKT TTL 7447	DIP.16 N BCD-7SEG DEC/DRV/OC	510074470
XU1-6	14 DIP RIGHT ANGLE SOCKET		820101710

Table 7—5. Model 1260A A11A2 Assembly Connector Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
A2	CONN HSNG,MALE 2P W/O	2 PIN	650910502
P3	CONN HSNG,MALE 2P W/O	2 PIN	650910502

Table 7—6. Model 1260A Loop Resistance Assembly A11A3 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
DS1-2	MINI GB-13A,9 PIN TUB.SKT		730100101
R1	RESISTOR WIRE-W 50 R	RES.012 N 3W 1%	210350091
R2	RESISTOR WIRE-W 100 R	RES.012 N 3W 1%	210310001
R3	RESISTOR WIRE-W 50 R	RES.012 N 3W 1%	210350091
R4	RESISTOR WIRE-W 100 R	RES.012 N 3W 1%	210310001
R5-6	RESISTOR WIRE-W 200 R	RES.012 N 3W 1%	210320001

Table 7—6. (Cont'd.)

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
R7	RESISTOR WIRE-W 400 R	RES.012 N 3W 1%	210340001
R8	RESISTOR WIRE-W 800 R	RES.012 N 3W 1%	210380001
R9	RESISTOR WIRE-W 400 R	RES.012 N 3W 1%	210340001
R10	RESISTOR WIRE-W 800 R	RES.012 N 3W 1%	210380001
R11-12	RESISTOR WIRE-W 1.6 K	RES.012 N 3W 1%	210316011

Table 7—7. Model 1260A Line Leak Assembly A11A4 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
C1	CAPACITR M-P-ESTR 2.16 UF	CAP.094 N 400V 2%	335321640
CR1	DIODE RECTIFER 1N4004	DIO.002 400V SI 1.0A	560040040
F1-2	FUSE 3AG	1A 250V	863100400
K1	RELAY,MERC.WET,PC 2C BIPL	12V	604104501
R1	TRIM-POT CERM-1ST 500 R	VRES.001 P 3/4W 10% END-ADJ	232505011
R2	RESISTOR MTL-FILM 4.42 K	RES.001 P 1/8W 1% 100PPMRN55	220244211
R3	RESISTOR MTL-FILM 10.2 K	RES.001 P 1/8W 1% 100PPMRN55	220210221
R4	RESISTOR MTL-FILM 600 R	RES.001 N 1/8W 1% 100PPMRN55	220260001
R5	RESISTOR MTL-FILM 15.0 K	RES.001 P 1/8W 1% 100PPMRN55	220215021
R6	RESISTOR MTL-FILM 20.5 K	RES.001 P 1/8W 1% 100PPMRN55	220220521

Table 7—8. Model 1260A Thumbwheel Assembly A11A5 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
A14	THUMBWHEEL SWITCH,8 SKT.		626801101
J1	HEDR,PC BD TO CONN	10 DIL	654003326
J2	HEDR WWP TO PCB 094 STR	50PIN	654000400

Table 7—9. Model 1260A Switch Assembly A11S20 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
CR1	TRANZORB 62 V		565500002
S20	4D-2CKT- 6POS NONSHORT	* *	626200200

Table 7—10. Model 1260A Front Panel Cable Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
J1	CONN,MOTOR MT, PIN	6 COND	650800100
P1	CONNECTOR MINI PC	20DILP	652001100
P2	CONN HSNG,MALE 2P W/O	2 PIN	650910502

Table 7—11. Model 1260A Switch Assembly A11S18 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
CR2-3	VARISTOR RY-57		565557000
S18	2C-2C-3C-3C		630101304

Table 7—12. Model 1260A Keypad Cable Assembly A11W1 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
P1-2	CONN,.100 MINI LATCH	13 SIL	652002023

Table 7—13. Model 1260A Shielded Cable Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
J3	CONN HSNG,MALE 9P W/O	9 PIN	650910509
J4	CONN HSNG,MALE 3P W/O	3 PIN	650910503
P4	CONN,.100 MINI LATCH	7 SIL	652002028

Table 7—14. Model 1260A Rear Panel Assembly A12 Overall Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
A10	POWER DISTR. A10		A126003020
C1-5	CAPACITR FEEDTHRU 1.0 NF	N 500V 20%	331101020
C6-8	CAPACITR ELECT-AL 8.0 UF	CAP.019 N 50V -10 +75%	300208051
K1	IC PC 2-.2K A-RELAY	48V	600300100
MOV1	VARISTOR V250LA		565500250
PS1	PWR SUPPLY,42-56VDC INPUT	5V-3A +-12V- .33	960100001
TB-1	TERMINAL BLOCK FEEDTHRU	4-POS.	850101001

Table 7—15. Model 1260A Power Distribution Assembly A12A10 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
C1	CAPACITR ELECT-AL 300 UF	CAP.003 N 100V	301403071
CR1-3	DIODE RECTIFER 1N5401	DIO.006 100V SI 3.0A	560054010

Table 7—16. Model 1260A Monitor Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
P4	CONN HSNG,FEMALE 3P W/O	3 PIN	650910103
P5	CONN HSNG,FEMALE 4P W/O	4 POS	650910104
P6	CONN HSNG,FEMALE 3P W/O	3 PIN	650910103
P7	CONN HSNG,FEMALE 2P W/O	2 PIN	650910102
P8	CONN HSNG,MALE 2P W/O	2 PIN	650910502

Table 7—17. Model 1260A Rear Panel Harness Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
P1	CONN,MOTOR MT, SOCKET	6 COND	650800204
P2	CONN HSNG,MALE 2P W/O	2 PIN	650910502
P3	CONN HSNG,FEMALE 2P W/O	2 PIN	650910102
P9	CONN HSNG,MALE 2P W/O	2 PIN	650910502

Table 7—18. Model 1260A Center Assembly Overall Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
A6	ANALOG RCVR BD ASSY A6		A126003022
A7	XMIT-REC INTF 96753 A7		A126000021
A8	BASIC BMSC PROCESSOR BD		A000100078
A9	1260A BMSC MEMORY A9		A126003014
J1	CONN HSNG,MALE 4P W/O	4 PIN	650910504
W4	1260A CPU CABLE W4		A126003023

Table 7—19. Model 1260A Analog Receiver Assembly A6 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
A6-J3	J3,PLUG ASSEMBLY		A126003034
C1	CAPACITR ELECT-TA 100 UF	CAP.039 N 10V 10%	310801070
C2	CAPACITR ELECT-TA 2.2 UF	CAP.042 N 35V 10%	310802250
C3-7	CAPACITR CERAMIC 10 NF	CAP.093 50V 00 Z5U	330701030
C8	CAPACITR ELECT-TA 4.7 UF	CAP.042 N 35V 20%	310804750
C9-13	CAPACITR CERAMIC 10 NF	CAP.093 50V 00 Z5U	330701030
C14	CAPACITR ELECT-TA 2.2 UF	CAP.042 N 35V 10%	310802250
C15-16	CAPACITR CERAMIC 10 NF	CAP.093 50V 00 Z5U	330701030
C17	CAPACITR CERAMIC 330 PF	CAP.082 1KV 10% Z5F	330003310
C18	CAPACITR ELECT-TA 10 UF	CAP.032 N 20V 10%	310301060
C19	CAPACITR CERAMIC 10 NF	CAP.093 50V 00 Z5U	330701030
C20	CAPACITR CERAMIC 10 PF	CAP.082 1KV 10% N330	330001000
C21	CAPACITR CERAMIC 39 PF	CAP.082 1KV 10% N330	330003900
C22	CAPACITR ELECT-TA 10 UF	CAP.032 N 20V 10%	310301060
C23	CAPACITR CERAMIC 10 NF	CAP.093 50V 00 Z5U	330701030
C24	CAPACITR ELECT-TA 10 UF	CAP.032 N 20V 10%	310301060
C25	CAPACITR CERAMIC 10 NF	CAP.093 50V 00 Z5U	330701030

Table 7—19. (Cont'd.)

REFERENCE DESIGNATOR	DESCRIPTION		EXT-DESC			N.E. PART NO.
C26	CAPACITR ELECT-TA	1.0 UF	CAP.036	N	35V 20%	310801050
C27-36	CAPACITR CERAMIC	10 NF	CAP.093		50V 00 Z5V	330701030
C37	CAPACITR ELECT-TA	820 NF	CAP.035	N	35V 10%	310308240
CR1	DIODE SIGNAL	1N4148	DIO.001		75V SI 4.0NS	560041480
CR2-5	DIODE RECTIFER	1N4004	DIO.002		400V SI 1.0A	560040040
CR6-14	DIODE SIGNAL	1N4148	DIO.001		75V SI 4.0NS	560041480
CR15	DIODE REFRENCE	2.4V	DIO.003		5% 1W IZ 20MA	562000240
CR16	DIODE SIGNAL	1N4148	DIO.001		75V SI 4.0NS	560041480
Q1	TRANSSTR BJT-PNP	2N3905	TO92.01		40V SI HFE50 200MA	552039050
Q2	TRANSSTR BJT-NPN	2N3903	TO92.01		40V SI HFE50 200MA	550039030
Q3-4	TRANSSTR BJT-NPN	MPSA06	TO92.01		80V SI HFE50 500MA	550000060
Q5-6	TRANSSTR BJT-PNP	MPSA56	TO92.01		80V SI HFE50 500MA	552000560
R1	RESISTOR CARBON	100 R	RES.001	P	1/4W 10%	200101016
R2	RESISTOR CARBON	33 K	RES.001	P	1/4W 10%	200103336
R3	RESISTOR CARBON	10 K	RES.001	P	1/4W 10%	200101036
R4	TRIM-POT CERM-18T	5.0 K	VRES.010	P	1/2W 10% TOP-ADJ	232705025
R5	RESISTOR CARBON	1.0 K	RES.003	P	1/2W 10%	200201026
R6-7	RESISTOR CARBON	510 R	RES.001	N	1/4W 5%	200105115
R8-9	RESISTOR CARBON	1.0 K	RES.001	P	1/4W 10%	200101026
R10	RESISTOR MTL-FILM	24.3 K	RES.001	P	1/8W 1% 100PPMRN55	220224321
R11	RESISTOR CARBON	100 K	RES.003	P	1/2W 10%	200201046
R12	RESISTOR CARBON	10 K	RES.001	P	1/4W 10%	200101036
R13-14	RESISTOR CARBON	10 R	RES.001	P	1/4W 10%	200101006
R15	RESISTOR CARBON	1.0 K	RES.001	P	1/4W 10%	200101026
R16	RESISTOR CARBON	100 R	RES.001	P	1/4W 10%	200101016
R17	RESISTOR CARBON	1.0 K	RES.001	P	1/4W 10%	200101026
R18	RESISTOR CARBON	51 K	RES.001	F	1/4W 10%	200105136
R19-20	RESISTOR CARBON	220 R	RES.001	P	1/4W 10%	200102216
R21	RESISTOR CARBON	100 K	RES.001	P	1/4W 10%	200101046
R22	RESISTOR CARBON	10 K	RES.001	P	1/4W 10%	200101036
R23-24	RESISTOR CARBON	1.0 K	RES.001	P	1/4W 10%	200101026
R25-26	RESISTOR CARBON	2.2 K	RES.001	P	1/4W 10%	200102226
R27	RESISTOR CARBON	24 K	RES.001	N	1/4W 5%	200102435
R28	RESISTOR CARBON	2.2 K	RES.001	P	1/4W 10%	200102226
R29	RESISTOR CARBON	1.0 K	RES.001	P	1/4W 10%	200101026
R30	RESISTOR CARBON	10 M	RES.001	P	1/4W 10%	200101066
R31	RESISTOR CARBON	220 R	RES.001	P	1/4W 10%	200102216
R32	RESISTOR CARBON	10 K	RES.001	P	1/4W 10%	200101036
R33	RESISTOR CARBON	1.0 K	RES.001	P	1/4W 10%	200101026
R34-41	RESISTOR CARBON	150 R	RES.001	P	1/4W 10%	200101516
R42	RESISTOR MTL-FILM	121 K	RES.001	P	1/8W 1% 100PPMRN55	220212131
R43	RESISTOR CARBON	1.0 M	RES.001	P	1/4W 10%	200101056
R44	RESISTOR CARBON	56 K	RES.001	P	1/4W 10%	200105636
R45-46	RESISTOR CARBON	10 K	RES.001	P	1/4W 10%	200101036
R47	RESISTOR CARBON	100 K	RES.001	P	1/4W 10%	200101046
R48-51	RESISTOR CARBON	10 K	RES.001	P	1/4W 10%	200101036
R52	RESISTOR CARBON	220 R	RES.001	P	1/4W 10%	200102216
R53	RESISTOR CARBON	3.3 K	RES.001	P	1/4W 10%	200103326
R54	RESISTOR CARBON	220 R	RES.001	P	1/4W 10%	200102216
R55	RESISTOR CARBON	10 K	RES.001	P	1/4W 10%	200101036
R56	RESISTOR CARBON	4.7 K	RES.001	P	1/4W 10%	200104726
R57	RESISTOR CARBON	47 R	RES.001	P	1/4W 10%	200104706
R58-61	RESISTOR CARBON	10 K	RES.001	P	1/4W 10%	200101036
S1	SWITCH,ROTARY MICRO DIP		1P		5POS	640001101
T1	TRANSFMR POT-CORE P.250V			N	S.400 OHMS 20%	420900101

Table 7—19. (Cont'd.)

REFERENCE DESIGNATOR	DESCRIPTION			EXT-DESC			N.E. PART NO.
U1	INT-CKT	DRIVER	75451	DIP.8	N	MEM & PERPH DUAL	510075451
U2-3	INT-CKT	TTL	7474	DIP.14	N	2 D-TYPE F/F	510074740
U4	INT-CKT	MLTVBRTR	9602		N	DUAL RETRIG/RESET	510096025
U5	INT-CKT	TTL	7401	DIP.14	N	4X2 IN NAND GATE/OC	510074010
U6-7	INT-CKT	OP-AMP	741	DIP.8	N		500057410
U8	INT-CKT	TTL	7402	DIP.14	N	4X2 IN NOR GATE	510074020
U9	INT-CKT	TTL	74393	DIP.14	N	2X4 BINARY RIP CNTR	510074393
U10	INT-CKT	TTL	7400	DIP.14	N	4X2 IN NAND GATE	510074000
U11	INT-CKT	TTL	7414	DIP.14	N	HEX SCHMITT TRIG	510007414
U12	INT-CKT	TTL	7474	DIP.14	N	2 D-TYPE F/F	510074740
U13-16	INT-CKT	OPTOCPLR	MCT2				515000200
U17	INT-CKT	CMOS	4069	DIP.14	P	HEX INVERTER	510004069
U18	INT-CKT	CMOS	4060BUF	DIP.16	P	14-STG RIPL BIN CNT	510004060
U19	INT-CKT	TTL	7404	DIP.14	N	HEX INVERTER	510074040
U20	INT-CKT	TTL	7400	DIP.14	N	4X2 IN NAND GATE	510074000
U21	INT-CKT	LS-TTL	74LS138	DIP.16	P	3-8 LINE DEC/DEMUX	510974138
U22-28	INT-CKT	TTL	74368	DIP.16	N	HEX INV 4-2BT /3S	510074368
U29-30	RESISTOR	NETWORK	15X10K	DIP 16		100V 2%	514500101
VR1	DIODE	REFRENCE	1N752A	DIO.001		5.6V 5% 500MW	562007520
VR2	DIODE	REFRENCE	1N748A	DIO.001		3.9V 5% 500MW	562007481
VR3	DIODE	REFRENCE	1N752A	DIO.001		5.6V 5% 500MW	562007520
VR4	INT-CKT	VOLT-REG	7905	TO220	P	FIXED NEG 1.5A	500079050
VR5	DIODE	REFRENCE	20V	DIO.003		1% 1W IZ 20MA	562002000
Y1	XTAL,.01% 0 TO+55,WIRE LD			PAR RES. 5 00 OHMS			919100002

Table 7—20. Model 1260A Analog Receiver Auxiliary Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION				EXT-DESC			N.E. PART NO.
C1	CAPACITR	POLYESTR	47	NF	CAP.043	P	100V 10%	320004730
C2	CAPACITR	POLYESTR	10	NF	CAP.043	P	100V 10%	320001030
C3-4	CAPACITR	CERAMIC	100	NF	CAP.088		50V 20% X5V	330801040
C5	CAPACITR	POLYESTR	100	NF	CAP.044	P	100V 10%	320001040
CR1-6	DIODE	SIGNAL	1N4148		DIO.001		75V SI 4.0NS	560041480
Q1	TRANSSTR	BJT-NPN	MPS6515		TO92.01		25V SI HFE250 0.1A	550065150
R1	RESISTOR	MTL-FILM	23.7	K	RES.001	P	1/8W 1% 100PPMRN55	220223721
R2	RESISTOR	MTL-FILM	20.0	K	RES.001	P	1/8W 1% 100PPMRN55	220220021
R3	RESISTOR	MTL-FILM	80.6	K	RES.001	P	1/8W 1% 100PPMRN55	220280621
R4	RESISTOR	MTL-FILM	6.81	K	RES.001	P	1/8W 1% 100PPMRN55	220268111
R5	RESISTOR	MTL-FILM	69.8	K	RES.001	P	1/8W 1% 100PPMRN55	220269821
R6	RESISTOR	CARBON	5.1	K	RES.001	N	1/4W 5%	200105125
R7	RESISTOR	MTL-FILM	49.9	K	RES.001	P	1/8W 1% 100PPMRN55	220249921
R8	RESISTOR	CARBON	5.1	K	RES.001	N	1/4W 5%	200105125
U1	INT-CKT	OP-AMP	741		DIP.8	P	GEN PURPOSE	500007412
U2	INT-CKT	CMOS	4538BUF		DIP.16	P	2X PRC MONO MLTIVI	510004538

Table 7—21. Model 1260A Transmitter and Receiver Interface Assembly A7 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION				EXT-DESC			N.E. PART NO.
C1-12	CAPACITR	CERAMIC	10	NF	CAP.093		50V 00 Z5V	330701030
C13	CAPACITR	ELECT-TA	4.7	UF	CAP.042	N	35V 20%	310804750
C14	CAPACITR	ELECT-TA	820	NF	CAP.035	N	35V 10%	310308240
C15	CAPACITR	CERAMIC	330	PF	CAP.082		1KV 10% Z5F	330003310
C16	CAPACITR	CERAMIC	470	PF	CAP.082		1KV 10% Z5F	330004710
C17	CAPACITR	CERAMIC	10	NF	CAP.093		50V 00 Z5V	330701030
C18	CAPACITR	CERAMIC	330	PF	CAP.082		1KV 10% Z5F	330003310
C19-21	CAPACITR	CERAMIC	10	NF	CAP.093		50V 00 Z5V	330701030
C22	CAPACITR	ELECT-TA	10	UF	CAP.032	N	20V 10%	310301060
C23	CAPACITR	CERAMIC	330	PF	CAP.082		1KV 10% Z5F	330003310
R1-13	RESISTOR	CARBON	10	K	RES.001	P	1/4W 10%	200101036
R14	RESISTOR	CARBON	100	R	RES.001	P	1/4W 10%	200101016
R15	RESISTOR	CARBON	62	K	RES.001	F	1/4W 10%	200106236
R16	RESISTOR	CARBON	3.0	K	RES.001	N	1/4W 5%	200103025
R17	RESISTOR	CARBON	33	K	RES.001	P	1/4W 10%	200103336
R18-19	RESISTOR	CARBON	47	K	RES.001	N	1/4W 5%	200104735
R20	RESISTOR	CARBON	1.0	K	RES.001	P	1/4W 10%	200101026
R21	RESISTOR	CARBON	47	K	RES.001	N	1/4W 5%	200104735
U1	INT-CKT	TTL	74367		DIP.16	N	HEX BUF 4-2BT /3S	510074367
U2	INT-CKT	TTL	7475		DIP.16	N	4 BI-STABLE LATCH	510074750
U3	INT-CKT	TTL	74197		DIP.14	N	PRESET BINARY CNTR	510074197
U4-5	INT-CKT	TTL	7475		DIP.16	N	4 BI-STABLE LATCH	510074750
U6	INT-CKT	TTL	74197		DIP.14	N	PRESET BINARY CNTR	510074197
U7-8	INT-CKT	TTL	7475		DIP.16	N	4 BI-STABLE LATCH	510074750
U9	INT-CKT	TTL	74197		DIP.14	N	PRESET BINARY CNTR	510074197
U10	INT-CKT	TTL	74367		DIP.16	N	HEX BUF 4-2BT /3S	510074367
U11	INT-CKT	TTL	7475		DIP.16	N	4 BI-STABLE LATCH	510074750
U12	INT-CKT	TTL	74197		DIP.14	N	PRESET BINARY CNTR	510074197
U13	INT-CKT	TTL	7404		DIP.14	N	HEX INVERTER	510074041
U14	INT-CKT	L-TTL	74L00		DIP.14	N	4X2 IN NAND GATE	510074001
U15	INT-CKT	TTL	7402		DIP.14	N	4X2 IN NOR GATE	510074020
U16-17	INT-CKT	LS-TTL	74LS138		DIP.16	P	3-8 LINE DEC/DEMUX	510974138
U18	INT-CKT	TTL	7474		DIP.14	N	2 D-TYPE F/F	510074740
U19-20	INT-CKT	TTL	74148		DIP.16	N	8-3 PRI-ENCODR	510074148
U21	INT-CKT	L-TTL	74L00		DIP.14	N	4X2 IN NAND GATE	510074001
U22-24	INT-CKT	MICRO-PR	8212				8BT I/O PORT	514001500
U25	INT-CKT	TTL	74125		DIP.14	N	4 BUS BUFFER/3S	510074125
U26-27	INT-CKT	TTL	74393		DIP.14	N	2X4 BINARY RIP CNTR	510074393
U28	INT-CKT	MLTVBRTR	9602			N	DUAL RETRIG/RESET	510096025
U29	INT-CKT	TTL	7474		DIP.14	N	2 D-TYPE F/F	510074740
U30	INT-CKT	MLTVBRTR	9602			N	DUAL RETRIG/RESET	510096025
U31-32	INT-CKT	TTL	7474		DIP.14	N	2 D-TYPE F/F	510074740
U33	INT-CKT	LS-TTL	74LS138		DIP.16	P	3-8 LINE DEC/DEMUX	510974138
U34	INT-CKT	MLTVBRTR	9602			N	DUAL RETRIG/RESET	510096025
U35	INT-CKT	TTL	7402		DIP.14	N	4X2 IN NOR GATE	510074020
U36	INT-CKT	L-TTL	74L00		DIP.14	N	4X2 IN NAND GATE	510074001
U37	INT-CKT	TTL	7414		DIP.14	N	HEX SCHMITT TRIG	510007414

Table 7—22. Model 1260A CPU Assembly A8 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC			N.E. PART NO.
C1-6	CAPACITR CERAMIC 10 NF	CAP.093		50V 00 Z5V	330701030
C7	CAPACITR CERAMIC 15 PF	CAP.082		1KV 10% N330	330001500
C8	CAPACITR ELECT-TA 4.7 UF	CAP.036	N	25V 10%	310004751
J2	HEDR,PC BD TO CONN	25 DIL			654003311
R1-2	RESISTOR CARBON 3.0 K	RES.001	N	1/4W 5%	200103025
R3	RESISTOR CARBON 4.7 K	RES.001	P	1/4W 10%	200104726
R4	RESISTOR CARBON 100 K	RES.001	P	1/4W 10%	200101046
R5	RESISTOR CARBON 4.7 K	RES.001	P	1/4W 10%	200104726
R6	RESISTOR CARBON 1.0 K	RES.001	P	1/4W 10%	200101026
R7	RESISTOR CARBON 3.0 K	RES.001	N	1/4W 5%	200103025
R19	RESISTOR CARBON 4.7 K	RES.001	P	1/4W 10%	200104726
S1	SWITCH,MOM,PC MTG	SPDT			635201401
U2	INT-CKT LS-TTL 74LS15	DIP.14	P	3X3 IN AND GATE /OC	510907415
U3	INT-CKT TTL 7400	DIP.14	N	4X2 IN NAND GATE	510074000
U4-6	INT-CKT TTL 74367	DIP.16	N	HEX BUF 4-2BT /3S	510074367
U7	INT-CKT MICRO-PR 8228			SYS CNTRL BUS DRVR	514001402
U8	INT-CKT MICRO-PR 8224			CLOCK GEN/DRIVER	514001401
U9	INT-CKT MICRO-PR 8080			NMOS +/-5,12V 8BT	514001400
XU7	SOCKET,IC,LOW PROFILE	28 DIP			820101501
XU8	SOCKET,IC	16DIP			820101703
XU9	SKT LSI PC	40DILP			820101400
Y1	CRYSTAL 18 MHZ				919100010

Table 7—23. Model 1260A Memory Assembly A9 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
A9	BMSC MEMORY E/W 3 SOCKETS		A000103079

Table 7—24. Model 1260A Cable Assembly W2 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
P1-2	CONN,FLAT CBL TO CARD EDG	2 X 25	654200050

Table 7—25. Model 1260A Cable Assembly W3 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
P1	CONN,FLAT CBL TO CARD EDG	2 X 25	654200050
P2	SKT W/W POST TO FL CABLE	50PIN	654000301

Table 7—26. Model 1260A Option Card Cage Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC		N.E. PART NO.
J1-2	EYELET,C.E. CONN	TYPE 1A	22 DUAL MIL BLWS	651701000

Table 7—27. Model 1260A Cable Assembly W4 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
P1-2	CONN,FLAT CBL TO CARD EDG	2 X 25	654200050
P3-4	SKT W/W POST TO FL CABLE	50PIN	654000300

Table 7—28. Model 1260A J3 Plug Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
J3	CONN HSNG,FEMALE 2P W/O	2 PIN	650910102

Table 7—29. Model 1260A Option Card Cage Harness Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
J3	CONN HSNG,MALE 3P W/O	3 PIN	650910503
J4	CONN HSNG,MALE 2P W/O	2 PIN	650910502
J5	CONN HSNG,FEMALE 2P W/O	2 PIN	650910102
P2	CONN HSNG,FEMALE 9P W/O	9 PIN	650910109
P3	CONN,.100 MINI LATCH	7 SIL	652002028

Table 7—30. SF Adapter Option 1260-10 Overall Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
A1	S.F. MOD. BD. A		A126010011
W1	1260A 16 DILP 3M CABLE		A126010012

Table 7—31. SF Adapter Board A Parts List.

REFERENCE DESIGNATOR	DESCRIPTION				EXT-DESC			N.E. PART NO.
C1	CAPACITR	ELECT-TA	2.2	UF	CAP.042	N	35V 10%	310802250
C2	CAPACITR	CERAMIC	100	NF	CAP.088		50V 20% X5V	330801040
C3	CAPACITR	CERAMIC	10	NF	CAP.088		50V 10% W5R	330801030
C4	CAPACITR	ELECT-TA	470	NF	CAP.036	N	50V 10%	310004741
C5	CAPACITR	CERAMIC	1.0	NF	CAP.088		50V 10% X7R	330801021
C6	CAPACITR	POLYSTYR	68	NF	CAP.023	N	100V 2%	321506830
C7-8	CAPACITR	ELECT-TA	10	UF	CAP.042	N	20V 20%	310801060
C9-10	CAPACITR	CERAMIC	100	NF	CAP.088		50V 20% X5V	330801040
C11	CAPACITR	SIL-MICA	680	PF		N	100V 5%	335006810
C12	CAPACITR	POLYESTR	39	NF	CAP.043	P	100V 10%	320003930
C13	CAPACITR	POLYPROP	2.7	NF	CAP.059	N	100V 1%	322902741
C14-15	CAPACITR	CERAMIC	100	NF	CAP.088		50V 20% X5V	330801040
C16	CAPACITR	POLYPROP	2.7	NF	CAP.059	N	100V 1%	322902741
C17	CAPACITR	CERAMIC	10	NF	CAP.088		50V 10% W5R	330801030
C18	CAPACITR	CERAMIC	82	PF	CAP.082		1KV 10% N3300	330008200
C19-20	CAPACITR	ELECT-NP	100	UF	CAP.004	N	150V -10 +100% N-P	301301072
CR1	DIODE	SIGNAL	1N4152		DIO.001		40V SI 4.0NS	560041520
CR3	DIODE	SIGNAL	1N4148		DIO.001		75V SI 4.0NS	560041480
CR4	DIODE	RECTIFER	1N4003		DIO.002		200V SI 1.0A	560040030
CR5	VARISTOR		V150ZA					565500150
CR7	DIODE	SIGNAL	1N4152		DIO.001		40V SI 4.0NS	560041520
CR8-9	DIODE	REFRENCE	1N752A		DIO.001		5.6V 5% 500MW	562007520
CR10	VARISTOR		V150ZA					565500150
CR11	DIODE	REFRENCE	1N970A		DIO.001		24V 10% 500MW	562007690
CR12	DIODE	SIGNAL	1N4152		DIO.001		40V SI 4.0NS	560041520
CR13	DIODE	REFRENCE	1N751A		DIO.001		5.1V 5% 500MW	562007511
CR14-16	DIODE	SIGNAL	1N4152		DIO.001		40V SI 4.0NS	560041520
CR18-21	DIODE	SIGNAL	1N4152		DIO.001		40V SI 4.0NS	560041520
CR22	DIODE	SIGNAL	1N4148		DIO.001		75V SI 4.0NS	560041480
E1-2	PROTECTR							566009020
J1	SKT,LO-PROFL,IN-LINE				16 DIP			820101100
J2	HEDR,PC BD TO CONN				9 DIL			654003327
K1	RELAY,PC,DPDT,LOW PROF.						1A 12V	604800500
Q1	TRANSSTR	BJT-PNP	MPS6518		TO92.01		40V SI HFE150 0.1A	550065180
Q2	TRANSSTR	BJT-PNP	MPSA56		TO92.01		80V SI HFE50 500MA	552000560
Q3	TRANSSTR	JFET-NCH	T1S73		TO92-M		30V SI	554000730
R1	RESISTOR	CARBON	330	R	RES.003	P	1/2W 10%	200203316
R2	RESISTOR	CARBON	100	K	RES.001	P	1/4W 10%	200101046
R3	RESISTOR	WIRE-W	600	R	RES.012	N	3W 1%	210360001
R4	TRIM-POT	CERM-18T	100	R	VRES.010	P	1/2W 10% TOP-ADJ	232701014
R5	RESISTOR	MTL-FILM	226	R	RES.001	P	1/8W 1% 100PPMRN55	220222601
R6	RESISTOR	MTL-FILM	182	K	RES.001	P	1/8W 1% 100PPMRN55	220218231
R7	RESISTOR	CARBON	820	K	RES.001	P	1/4W 10%	200108246
R8	RESISTOR	MTL-FILM	45.3	K	RES.001	P	1/8W 1% 100PPMRN55	220245321
R9	RESISTOR	MTL-FILM	80.6	K	RES.001	P	1/8W 1% 100PPMRN55	220280621
R10	RESISTOR	CARBON	100	K	RES.001	P	1/4W 10%	200101046
R11-12	RESISTOR	CARBON	39	K	RES.001	P	1/4W 10%	200103936

Table 7–31. (Cont'd.)

REFERENCE DESIGNATOR	DESCRIPTION				EXT-DESC					N.E. PART NO.
R13	RESISTOR	MTL-FILM	5.49	K	RES.001	P	1/8W	1%	100PPMRN55	220254911
R14	RESISTOR	CARBON	6.8	K	RES.001	P	1/4W	10%		200106826
R15	RESISTOR	CARBON	100	K	RES.001	P	1/4W	10%		200101046
R16	TRIM-POT	CERM-18T	500	R	VRES.010	P	1/2W	10%	TOP-ADJ	232705014
R17	RESISTOR	MTL-FILM	24.6	K	RES.001	N	1/8W	1%	100PPMRN55	220224621
R18	RESISTOR	MTL-FILM	47.5	K	RES.001	N	1/8W	1%	25PPM-RN55	221047521
R19	RESISTOR	MTL-FILM	17.4	K	RES.001	P	1/8W	1%	100PPMRN55	220217421
R20	TRIM-POT	CERM-18T	5.0	K	VRES.010	P	1/2W	10%	TOP-ADJ	232705025
R21	RESISTOR	MTL-FILM	49.9	K	RES.001	P	1/8W	1%	100PPMRN55	220249921
R22	RESISTOR	CARBON	4.7	K	RES.003	P	1/2W	10%		200204726
R23	RESISTOR	MTL-FILM	226	R	RES.001	P	1/8W	1%	100PPMRN55	220222601
R24	RESISTOR	CARBON	47	K	RES.001	P	1/4W	10%		200104736
R25	RESISTOR	CARBON	10	K	RES.001	P	1/4W	10%		200101036
R26	RESISTOR	CARBON	100	K	RES.001	P	1/4W	10%		200101046
R27	RESISTOR	CARBON	47	K	RES.001	P	1/4W	10%		200104736
R28	RESISTOR	CARBON	6.8	K	RES.004	N	1W	10%		200306826
R29	RESISTOR	CARBON	47	K	RES.001	P	1/4W	10%		200104736
R30-31	RESISTOR	MTL-FILM	18.2	K	RES.001	P	1/8W	1%	100PPMRN55	220218221
R32	RESISTOR	CARBON	1.0	M	RES.001	P	1/4W	10%		200101056
R33	RESISTOR	CARBON	100	K	RES.001	P	1/4W	10%		200101046
R34	RESISTOR	MTL-FILM	18.2	K	RES.001	P	1/8W	1%	100PPMRN55	220218221
R35	RESISTOR	MTL-FILM	9.09	K	RES.001	P	1/8W	1%	100PPMRN55	220290911
R36	RESISTOR	MTL-FILM	22.1	K	RES.001	P	1/8W	1%	100PPMRN55	220222121
R37	RESISTOR	MTL-FILM	2.15	K	RES.001	P	1/8W	1%	100PPMRN55	220221511
R38	TRIM-POT	CERM-18T	100	R	VRES.010	P	1/2W	10%	TOP-ADJ	232701014
R39-42	RESISTOR	MTL-FILM	2.26	K	RES.001	P	1/8W	1%	100PPMRN55	220222611
R43	TRIM-POT	CERM-18T	10	K	VRES.010	P	1/2W	10%	TOP-ADJ	232701035
R44	RESISTOR	MTL-FILM	34.8	K	RES.001	P	1/8W	1%	100PPMRN55	220234821
R45	RESISTOR	MTL-FILM	6.81	K	RES.001	P	1/8W	1%	100PPMRN55	220268111
R46	RESISTOR	CARBON	100	K	RES.001	P	1/4W	10%		200101046
R47	RESISTOR	MTL-FILM	78.7	K	RES.001	P	1/8W	1%	100PPMRN55	220278721
R48	RESISTOR	CARBON	100	K	RES.001	P	1/4W	10%		200101046
R49	RESISTOR	MTL-FILM	196	K	RES.001	P	1/8W	1%	100PPMRN55	220219631
R50-51	RESISTOR	MTL-FILM	24.6	K	RES.001	N	1/8W	1%	100PPMRN55	220224621
R52	RESISTOR	MTL-FILM	196	K	RES.001	P	1/8W	1%	100PPMRN55	220219631
R53	RESISTOR	MTL-FILM	9.76	K	RES.001	P	1/8W	1%	100PPMRN55	220297611
R54	RESISTOR	CARBON	1.0	M	RES.001	P	1/4W	10%		200101056
R55	RESISTOR	MTL-FILM	4.99	K	RES.001	P	1/8W	1%	100PPMRN55	220249911
T1	TRANSFMR		P50KCT		XFMR.014	N	S50KCT 200-10KHZ			400101100
T2	TRANSFMR	COUPLING	P600CT		XFMR.019	N	S600CT 200-20KHZ PC			400300201
U1	INT-CKT	CMOS	4538BUF		DIP.16	P	2X PRC MONO MLTIVI			510004538
U2	INT-CKT	COMPARTR	339		DIP.14	P	QUAD 5-36V			500000339
U3-4	INT-CKT	OP-AMP	1458		8PD1L	P	DUAL 741C			500001458
U5	INT-CKT	OPTOCPLR	8050							515000103
U6	INT-CKT	OP-AMP	1458		8PD1L	P	DUAL 741C			500001458

Table 7—32. SF Adapter Board B Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
C1-2	CAPACITR CERAMIC 100 NF	CAP.088 50V 20% X5V	330801040
C3-4	CAPACITR M-P-PROP 47 NF	N 150V 1%	322504730
C5-7	CAPACITR CERAMIC 1.0 UF	CAP.037 50V 20% Y5V	330801050
C8	CAPACITR ELECT-NP 35 UF	CAP.029 N 15V -10 +100% N-P	301303560
CR1-5	DIODE SIGNAL 1N4152	DIO.001 40V SI 4.0NS	560041520
J1	HEDR,R/A,PC BD TO CONN	13 SIP L WR HALF	654003123
J1	HEDR,R/A,PC BD TO CONN.	13 SIP	654003223
J2	SKT,LO-PROFL,IN-LINE	16 DIP	820101100
Q1	TRANSSTR BJT-NPN MPS6515	TO92.01 25V SI HFE250 0.1A	550065150
Q2	TRANSSTR JFET-NCH VCR4N	TO18 15V SI	554000003
Q3-4	TRANSSTR JFET-NCH T1S73	TO92-M 30V SI	554000730
Q5	TRANSSTR JFET-NCH T1S75	TO92-M 30V SI	554000750
Q6	TRANSSTR BJT-PNP MPS6518	TO92.01 40V SI HFE150 0.1A	550065180
R1	TRIM-POT CERM-18T 100 R	VRES.010 P 1/2W 10% TOP-ADJ	232701014
R2	RESISTOR MTL-FILM 100 R	RES.001 P 1/8W 1% 100PPMRN55	220210001
R3	RESISTOR MTL-FILM 11.8 K	RES.001 P 1/8W 1% 100PPMRN55	220211821
R4	RESISTOR MTL-FILM 10.0 K	RES.001 P 1/8W 1% 100PPMRN55	220210021
R5	RESISTOR MTL-FILM 68.1 R	RES.001 P 1/8W 1% 100PPMRN55	220268191
R6	RESISTOR MTL-FILM 1.30 K	RES.001 P 1/8W 1% 100PPMRN55	220213011
R7	RESISTOR MTL-FILM 196 R	RES.001 P 1/8W 1% 100PPMRN55	220219601
R8	TRIM-POT CERM-18T 200 R	VRES.010 P 1/2W 10% TOP-ADJ	232702017
R9	RESISTOR MTL-FILM 205 R	RES.001 P 1/8W 1% 100PPMRN55	220220501
R10	RESISTOR MTL-FILM 162 R	RES.001 P 1/8W 1% 100PPMRN55	220216201
R11	RESISTOR MTL-FILM 127 R	RES.001 P 1/8W 1% 100PPMRN55	220212701
R12	RESISTOR MTL-FILM 15.8 R	RES.001 P 1/8W 1% 100PPMRN55	220215891
R13	RESISTOR MTL-FILM 110 R	RES.001 P 1/8W 1% 100PPMRN55	220211001
R14	RESISTOR MTL-FILM 1.27 K	RES.001 P 1/8W 1% 100PPMRN55	220212711
R15	TRIM-POT CERM-18T 100 R	VRES.010 P 1/2W 10% TOP-ADJ	232701014
R16	RESISTOR MTL-FILM 634 R	RES.001 P 1/8W 1% 100PPMRN55	220263401
R17	RESISTOR MTL-FILM 129.8 R	RES.001 F 1/8W 1% 100PPMRN55	220212901
R18	RESISTOR MTL-FILM 4.99 K	RES.001 P 1/8W 1% 100PPMRN55	220249911
R19	RESISTOR MTL-FILM 54.9 R	RES.001 P 1/8W 1% 100PPMRN55	220254991
R20	RESISTOR MTL-FILM 48.7 R	RES.001 P 1/8W 1% 100PPMRN55	220248791
R21	RESISTOR MTL-FILM 2.74 K	RES.001 P 1/8W 1% 100PPMRN55	220227411
R22	RESISTOR MTL-FILM 511 R	RES.001 P 1/8W 1% 100PPMRN55	220251101
R23	RESISTOR MTL-FILM 17.8 R	RES.001 P 1/8W 1% 100PPMRN55	220217891
R24	RESISTOR MTL-FILM 432 R	RES.001 P 1/8W 1% 100PPMRN55	220243201
R25	RESISTOR MTL-FILM 19.1 R	RES.001 P 1/8W 1% 100PPMRN55	220219191
R26	RESISTOR MTL-FILM 887 R	RES.001 P 1/8W 1% 100PPMRN55	220288701
R27	TRIM-POT CERM-18T 10 K	VRES.010 P 1/2W 10% TOP-ADJ	232701035
R28	RESISTOR MTL-FILM 37.4 K	RES.001 P 1/8W 1% 100PPMRN55	220237421
R29	RESISTOR CARBON 39 K	RES.001 P 1/4W 10%	200103936
R30	RESISTOR MTL-FILM 34.8 K	RES.001 P 1/8W 1% 100PPMRN55	220234821
R31	RESISTOR MTL-FILM 2.74 K	RES.001 P 1/8W 1% 100PPMRN55	220227411
R32	RESISTOR MTL-FILM 3.74 K	RES.001 P 1/8W 1% 100PPMRN55	220237411
R33-34	RESISTOR CARBON 470 K	RES.001 P 1/4W 10%	200104746
R35	RESISTOR CARBON 1.0 M	RES.001 P 1/4W 10%	200101056
R36	RESISTOR MTL-FILM 44.2 R	RES.001 P 1/8W 1% 100PPMRN55	220244291
R37	RESISTOR MTL-FILM 38.3 R	RES.001 P 1/8W 1% 100PPMRN55	220238391
R38	RESISTOR MTL-FILM 2.94 K	RES.001 P 1/8W 1% 100PPMRN55	220229411
R39	RESISTOR MTL-FILM 22.6 R	RES.001 P 1/8W 1% 100PPMRN55	220222691
R40	RESISTOR MTL-FILM 1.262 K	RES.001 F 1/8W 1% 100PPMRN55	220212611
R41	RESISTOR MTL-FILM 25.5 R	RES.001 P 1/8W 1% 100PPMRN55	220225591
R42	RESISTOR MTL-FILM 100 K	RES.001 P 1/8W 1% 100PPMRN55	220210031
R43	RESISTOR MTL-FILM 90.9 K	RES.001 P 1/8W 1% 100PPMRN55	220290921
R44	RESISTOR MTL-FILM 4.99 K	RES.001 P 1/8W 1% 100PPMRN55	220249911
R45	RESISTOR MTL-FILM 34.8 R	RES.001 P 1/8W 1% 100PPMRN55	220234891

Table 7—32. (Cont'd.)

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
R46	RESISTOR MTL-FILM 30.9 R	RES.001 P 1/8W 1% 100PPMRN55	220230991
R47	RESISTOR MTL-FILM 619 R	RES.001 P 1/8W 1% 100PPMRN55	220261901
R48	RESISTOR MTL-FILM 26.7 R	RES.001 P 1/8W 1% 100PPMRN55	220226791
R49	RESISTOR MTL-FILM 100 K	RES.001 P 1/8W 1% 100PPMRN55	220210031
R50	RESISTOR MTL-FILM 12.1 K	RES.001 P 1/8W 1% 100PPMRN55	220212121
R51	TRIM-POT CERM-18T 50 K	VRES.010 P 1/2W 10% TOP-ADJ	232705034
R52	RESISTOR CARBON 1.0 M	RES.001 P 1/4W 10%	200101056
R53	RESISTOR CARBON 100 K	RES.001 P 1/4W 10%	200101046
R54	RESISTOR MTL-FILM 28.0 K	RES.001 P 1/8W 1% 100PPMRN55	220228021
R55	RESISTOR MTL-FILM 2.10 K	RES.001 P 1/8W 1% 100PPMRN55	220221011
R56	RESISTOR MTL-FILM 100 K	RES.001 P 1/8W 1% 100PPMRN55	220210031
R57-58	RESISTOR CARBON 100 K	RES.001 P 1/4W 10%	200101046
R59	RESISTOR CARBON 1.0 M	RES.001 P 1/4W 10%	200101056
R60	RESISTOR MTL-FILM 49.9 K	RES.001 P 1/8W 1% 100PPMRN55	220249921
R61	RESISTOR MTL-FILM 90.9 K	RES.001 P 1/8W 1% 100PPMRN55	220290921
R62	RESISTOR CARBON 1.0 K	RES.001 P 1/4W 10%	200101026
S1	DIP SWITCH,8 POSITION		640001000
U1	INT-CKT OP-AMP 318	N SINGLE HIGH SPEED	500000318
U2	INT-CKT CMOS 4093BUF	DIP.14 P 4X2 IN NAND SCHM TR	510004093
U3	INT-CKT OP-AMP 741	DIP.8 P GEN PURPOSE	500007412
U4	INT-CKT OP-AMP 1458	8PD1L P DUAL 741C	500001458

Table 7—33. SF Adapter Front Panel Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
DS-1	DIODE LED-RED		564500802
J1-3	JACK,TEL,SCHEM 15		650403300
W2	1260A FRONT PNL CABLE		A126010013
W3	LOWER LEVEL CABLE (W3)		A126010015

Table 7—34. SF Adapter Cable Assembly W1 Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
P1-2	PLUG,FL CABLE TO PC SKT	16PD/L	653800500

Table 7—35. SF Adapter Front Panel Cable Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
P4	HOUSING,MINI-LATCH	18 POS	652001900
S2	ON-OFF-ON	3PDT 5A 28V	620401300

Table 7—36. AC Power Supply Option 1260-11 Overall Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC		N.E. PART NO.
A1	1260A AC OPT. PWR SUPPLY			9126011011
F1-2	FUSE 3AG	2A	250V	863100600
F3	FUSE, SLO-BLO	2A	250V	863101700
J1	RECEPT,PANEL,BLK PLASTIC	3-PIN	6A 250V	652201700
J2	CONN HSNG,FEMALE 2P W/O	2 PIN		650910102
Q1	TRANSSTR BJT-NPN 2N3055	TO3.01	60V SI HFE20 15A	550030550
S1	DPDT LOCKING	3A	125V	645500200
T1	TRANSFMR POWER P234VSP	N S44V		420500401
XF1-2	FUSEHOLDER,3AG PANEL			863000100
XF3	FUSEHOLDER 3AG CHASSIS			863000200

Table 7—37. AC Power Supply Regulator Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC		N.E. PART NO.
C1	CAPACITR ELECT-AL 1000 UF	CAP.005 P	75V -10 +75%	300001081
CR1	DIODE REFRENCE 1N5359B	DIO.008	24V 5% 5W	562053592
CR2-5	DIODE RECTIFER 1N4005	DIO.002	600V SI 1.0A	560040050
MP1	HEATSINK,PC MTG,TO-220			890000801
Q2	TRANSSTR BJT-NPN MJE344	TO126.01	200V SI HFE20	550000344
R1	TRIM-POT CERM-1ST 2.0 K	VRES.001 P	3/4W 10% END-ADJ	232502020
R2	RESISTOR CARBON 2.2 K	RES.003 N	1/2W 5%	200202225
R3	RESISTOR CARBON 3.0 K	RES.003 N	1/2W 5%	200203025
R4	RESISTOR CARBON 4.7 K	RES.003 N	1/2W 5%	200204725
R5	RESISTOR WIRE-W 400 R	RES.004 N	3W 5%	210304015
R6	RESISTOR WIRE-W 1.0 R	RES.004 N	3W 5%	210300105

Table 7—38. Local Pulse Repeating Artline Option 1260-12 Overall Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
DS1	DIODE LED-RED		564500802
R1	RESISTOR WIRE-W 25 R	RES.501 N 5W 5%	210902501
R2	RESISTOR WIRE-W 50 R	RES.501 N 5W 5%	210905001
R3	RESISTOR WIRE-W 100 R	RES.502 N 10W 5%	210901011
R4	RESISTOR WIRE-W 200 R	RES.502 N 10W 5%	210902011
R5	RESISTOR WIRE-W 400 R	RES.502 N 10W 5%	210904011
R6	RESISTOR WIRE-W 800 R	RES.501 N 5W 5%	210908011
R7	RESISTOR WIRE-W 1.6 K	RES.501 N 5W 5%	210901621
R8	RESISTOR WIRE-W 25 R	RES.501 N 5W 5%	210902501
R9	RESISTOR WIRE-W 50 R	RES.501 N 5W 5%	210905001
R10	RESISTOR WIRE-W 100 R	RES.502 N 10W 5%	210901011

Table 7—38. (Cont'd.)

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
R11	RESISTOR WIRE-W 200 R	RES.502 N 10W 5%	210902011
R12	RESISTOR WIRE-W 400 R	RES.502 N 10W 5%	210904011
R13	RESISTOR WIRE-W 800 R	RES.501 N 5W 5%	210908011
R14	RESISTOR WIRE-W 1.6 K	RES.501 N 5W 5%	210901621

Table 7—39. Artline Oscillator Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
C1	CAPACITR ELECT-TA 10 UF	CAP.042 N 25V 10%	310801061
CR1	DIODE REFRENCE 1N5357A	DIO.008 20V 10% 5W	562053571
J2A	HEDR,R/A,PC BD TO CONN	17 SIP L WR HALF	654003119
J2B	HEDR,R/A,PC BD TO CONN	17 SIP	654003219
Q1	TRANSSTR UNI-JNCT 2N4852	22A-01	556048520
R16	RESISTOR CARBON 4.7 K	RES.001 P 1/4W 10%	200104726
R17	RESISTOR CARBON 33 K	RES.001 P 1/4W 10%	200103336
R18	RESISTOR WIRE-W 1.2 K	RES.013 N 3W 10%	210301226
R19	RESISTOR CARBON 220 R	RES.001 P 1/4W 10%	200102216
S1A-S1H	SWITCH,PB,SPECIAL PB79656	8SWITCH	635600101

Table 7—40. Artline Cable Assembly Parts List.

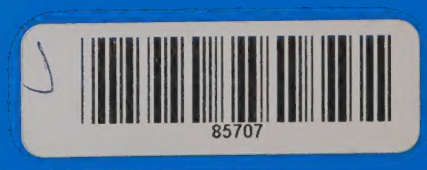
REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
P2	HOUSING	34DILP	652001520

Table 7—41. Monitor Adapter Option 1260—13 Front Panel Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
J1-2	JACK,TEL,SCHEM 15		650403300
S1	2D CONTACTS		630101302

Table 7—42. Monitor Adapter Resistor Assembly Parts List.

REFERENCE DESIGNATOR	DESCRIPTION	EXT-DESC	N.E. PART NO.
R1	RESISTOR WIRE-W 900 R	RES.014 N 5W 5%	210409015



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